ISSN: 2584-0495 Vol. 2, Issue 8, pp. 1112-1117

International Journal of Microsystems and IoT

ISSN: (Online) Journal homepage: https://www.ijmit.org

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Cite as: Jahnavi, E., Geethamrutha, U., Rehman, B. K., Chandrasekhar, E., & Chandrasekhar, P. (2024). Design of 4-bit Binary Weighted DAC in 180nm CMOS Technology. International Journal of Microsystems and IoT, 2(8), 1112-1117. https://doi.org/10.5281/zenodo.13709786

Published online: 20 August 2024

DOI: https://doi.org/10.5281/zenodo.13709786

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Design of 4-bit Binary Weighted DAC in 180nm CMOS Technology

E. Jahnavi, U. Geethamrutha, B. Khaleelu Rehman, E. Chandrasekhar and P. Chandrasekhar

Department of Electronics and Communication Engineering, Chaitanya Bharathi Institute of Technology, Hyderabad, India

ABSTRACT

In this paper, a method for implementing 4-bit binary weighted digital to analog converterr using cadence virtuoso 180nm technology is presented. The presented DAC is designed at 1.8v power supply. Primarily a differential amplifier of gain 32.86db is followed by an operational amplifier of gain 56.90 db is designed using CMOS technology. A High gain operational amplifier helps in achieving better linearity and reduced distortions. The designing of this DAC involves creating transistor level schematic design followed by simulation using transient analysis. DAC's serve as fundamental building blocks in various applications like Audio and communication Systems.

KEYWORDS

DAC- Digital to analog converter, Amplifier,
CMOS, Resolution., Transient analysis, Nyquist Rate

1. INTRODUCTION

Data converters are essential components in electronics for various applications. These data converters are classified into two types, Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC). Digital to analog converter is a device that converts digital signal to continuous analog signal. Many electronic systems require analog signals for various purposes, such as motor control, audio generation and interfacing with analog sensors which enablee these systems to operate effectively. Binary weighted DAC and R-2R DAC [18] are binary scaled converters which come under Nyquist Rate D/A converters. Binary weighted DAC consists of series of resistor networks that are connected to an Operational Amplifier in inverting adder circuit. R-2R DAC consists of r-2r ladders with resistance ratio of 2, independent of number of bits N.

The main building block of DAC is two stage operational Amplifier which comprise of differential amplifier in the primary stage followed by common source amplifier. Opamp is a DC coupled high gain voltage amplifier. It has two inputs inverting(-) and non-inverting(+) and a single output which amplifies the difference of two inputs. Operational amplifiers provide voltage amplification, signal conditioning and voltage references which helps in the accuracy of conversion. The feedback control of Opamp helps for cancellation of noise generated during conversion of signals.

Programmable Gain Amplifiers, or PGA, which have the gain options internal and can be digitally controlled.

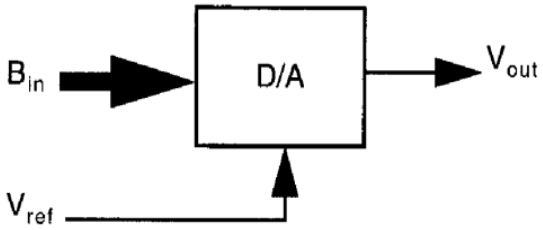


Fig. 1 Block diagram of D/A Converter [1]

The basic operation of DAC is, the digital input signal controls the switches which are connected to either reference voltage or ground. The respective network of DAC combines with current source to produce the analog output. The significance of inbuilt DACs in microcontrollers lies in their ability to provide efficient and cost-effective means of generating analog signals for various applications. They simplify design, reduce power consumption, and offer precision, making them valuable in a wide range of electronic systems. Binary weighted DAC has advantages of low propagation delay and fast settling time which makes the conversion speed faster and also easier scaling resulting in better resolution.

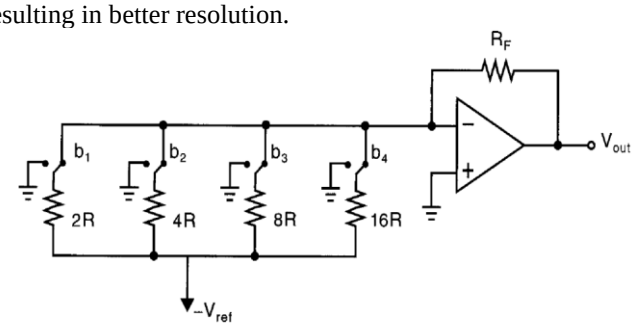


Fig. 2 4-Bit Binary Weighted DAC [1]

2. LITERATURE SURVEY

In the literature of Data Converters, Digital to Analog has a great significance. In the paper [18] DAC of 8 bit based on R-2R ladder is analyzed in terms of power consumption and implemented using CMOS Technology. In a similar way we have implemented binary weighted DAC in this paper in 180nm CMOS Technology. The fundamental block of DAC is Operational Amplifier, the papers [7], [8] and [9] presented Operational amplifiers in different technology's such as 90nm,180nm. The first stage of Op-amp is differential amplifier and it is discussed in [10] and [12] and the second stage is discussed in [19]. With these references a 4-bit binary weighted DAC is designed, and its power is analyzed.

Comparative study with other standard papers

Paper	Specifications
Reference paper[5]	Power=22mW Technology=180nm Approach= Current Steering
Reference paper[2]	Supply voltage=2.5V, Gain =30(in db)
Reference paper[21]	used NMOS, PMOS and Transmission gate.
Proposed paper	Technology=180nm Power=1.03mW Approach=Binary weighted Gain=56.90(in db)

3. METHODOLOGY

A. Design of Differential Amplifier

Differential Amplifier comprises two PMOS transistors in pull up structure and four NMOS transistors in pull down structure[6]. Current mirrors are used to provide stability in the current. The differential Amplifier has two inputs namely V_1 and V_2. The DC supply voltage V_{dd} is 1.8 V . The input V_1 is given a sine wave of magnitude 5mV and frequency 1KHz and other input V_2 is grounded for easier understanding. A capacitor of 10pF is linked at the output terminal. Bias current of 100uA is given to the circuit. The W/L ratio of each transistor (M_1, M_2, M_3, M_4, M_5, M_6)is 40.

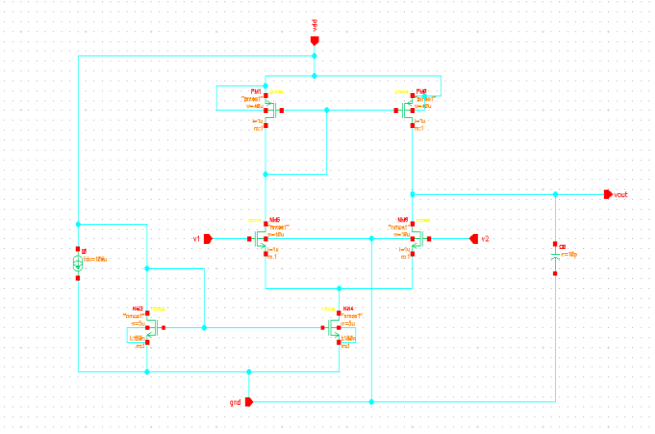


Fig. 3 Schematic of Differential Amplifier

B . Design of Operational Amplifier

Operational Amplifier consists of Differential amplifier in the primary stage which is followed by a common source amplifier to increase the gain and gives high yield voltage swing. In CMOS logic of Operational amplifier we have three PMOS transistors M_3, M_4, M_6 in pull up structure and remaining five NMOS transistors in pull down structure[2]. Similar to the differential amplifier it has two inputs V^+ and V^-. The DC supply voltage V_{dd} is 1.8 V . The input V^+ is given a sine wave of magnitude 1mV and frequency 10KHz and other input V^- is grounded for easier understanding. The compensation capacitance(C_c) of 800fF is used to increase frequency response and stability[19] and [20]. Current source of 20uA is connected in between V_{dd} and M_8. W/L ratio of the transistors M_1, M_2, M_5, M_6, M_7, M_8 is 16.6 and M_3, M_4 is 11.1.

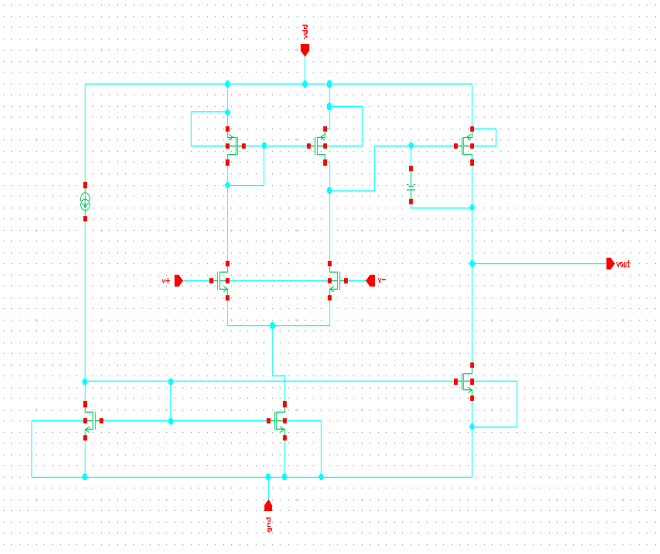


Fig. 4 Schematic of Operational Amplifier.

C . Design of 4-bit Binary Weighted DAC

In Binary weighted DAC resistors are connected between reference voltage V_{ref} and ground through switches[3]. If the binary input is high the resistor will be

connected to V_{ref} and if the input is low, it will be connected to the ground. For 4-bit DAC the resistor to current ratio ranges from 2^1 to 2^4. Binary weighted DAC offers high conversion speed but also consumes large power and complexity of the circuit becomes complicated as number of bits increase.

The designed 4-bit binary weighted DAC has four inputs d_1, d_2, d_3, d_4 which are given with a dc pulse signal of magnitude 1V. The resistor network R_0(2 KΩ) , R_1 (4 KΩ), R_2(8 KΩ), R_4(16 KΩ) and feedback (-ve) resistor R_3(1 KΩ) are connected to the inverting terminal of the operational amplifier. The DC supply voltage V_{dd} is 1.8 V .The time period of DC pulse signals d_1 , d_2, d_3, d_4 are 10u,20u,40u and 80us respectively.

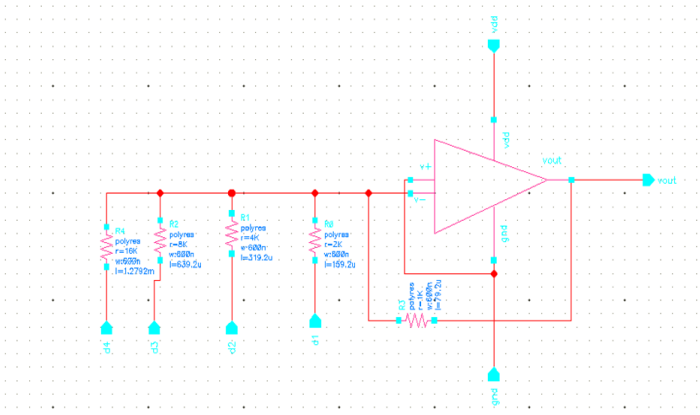


Fig. 5 Schematic of 4-bit Binary Weighted DAC

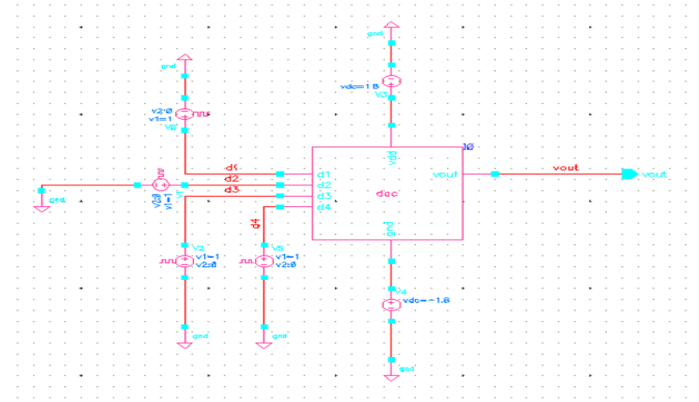


Fig. 6 Synthesis of 4-bit Binary Weighted DAC

4 . SIMULATION AND RESULTS

A. Differential Amplifier

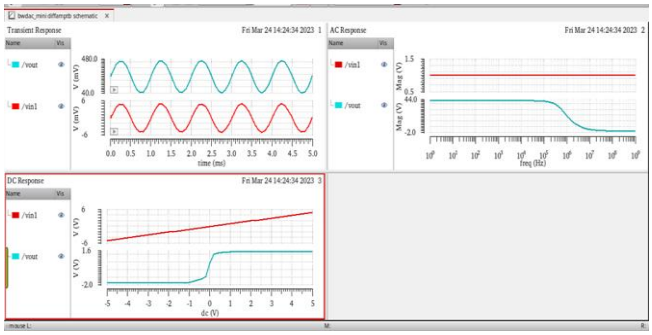


Fig. 7 Simulation of Differential Amplifier

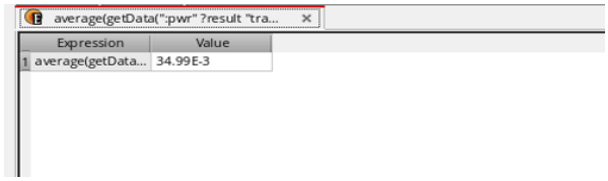


Fig. 8 Power consumption of Differential Amplifier

B. Operational Amplifier

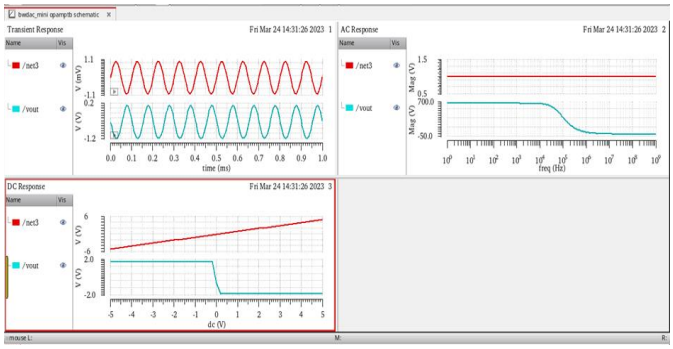


Fig. 9 : Simulation of Operational Amplifier

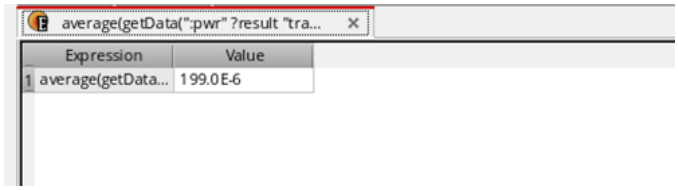


Fig. 10 : Power consumption of Operational Amplifier

C . 4-bit Binary Weighted DAC

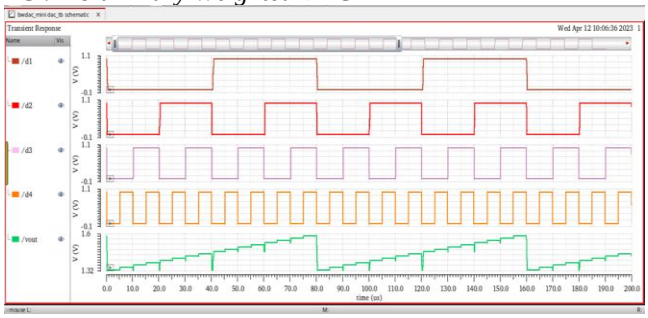


Fig. 11 : Simulation of 4-bit DAC

The output waveform of 4 bit binary weighted DAC is shown in figure 11. The four DC pulse signals of different frequencies are given as inputs to d1,d2,d3 and d4 of the circuit. The output waveform has 16 voltage levels. For binary input 0000, the DAC output is 0V. Similarly, for all possible combinations of inputs, we got respective output voltages.

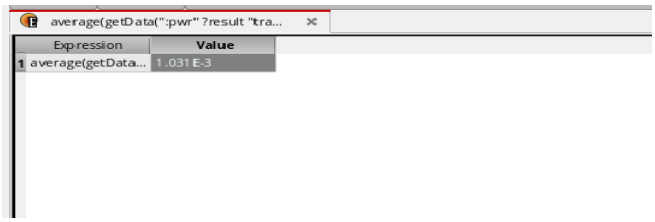


Fig. 12 Power consumption of 4-bit DAC

4. CALCULATIONS

Binary weighted DAC Vout=Vref*D/2^n

For 4 bit DAC,n=4

For binary input 0000,

Theoretical Vout=(1.8*0)/16=0V

Practical Vout= 0.1V

For binary input 1010,

Theoretical Vout=(1.8*10)/16=1.1.25V

Practical Vout=1.3V

For binary input 1111,

Theoretical Vout==(1.8*15)/16=1.68V

Practical Vout=1.53V

4-bit Binary weighted DAC is studied and simulated in Cadence Virtuoso using gpdk 180nm CMOS technology which involves design of 2-stage Operational Amplifier. CMOS technology has various advantages like large fanout, high noise margin and low propagation delay. This 2 stage Opamp is achieved by designing of differential amplifier as its first stage and common source amplifier as its second stage which consumed power of 199 µwatts and gain of 700. The power consumption of designed 4-bit Binary weighted Digital to analog Converter is 1.031 milli watts. These converters provide high resolution, fast conversion rates, and low power consumption. This Binary weighted DAC has various applications like Audio and Video processing, Telecommunications [13] and Medical Instrumentation [17] etc.

The proposed DAC can be enhanced by increasing number of bits which helps to achieve higher resolution of the analog signal. Future Binary weighted DACs aim to reduce power while maintaining performance making them suitable for battery-powered devices and energy efficient systems. They might also focus on robustness, reliability and automotive-specific requirements.

REFERENCES

[1] Saravanan, P., Deepakraj, R., Srreenandhini, K., & Krishnaveni, V. (2023). Design and Implementation of Operational Amplifiers with CMOS 180 nm Technology Node using gm/ID Methodology. In 2023 IEEE 20th India Council International Conference (INDICON) (706-712). IEEE.

[2] Kavyashree, C. L., Hemambika, M., Dharani, K., Naik, A. V., & Sunil, M. P. (2017, January). Design and implementation of two stage CMOS operational amplifier using 90nm technology. In 2017 International Conference on Inventive Systems and Control (ICISC) (pp. 1-4). IEEE.

[3] Sharma, B. P., Soni, A., Gupta, A., & Shekhar, C. (2023). Comparative Analysis of D/A Converter Architectures for SAR ADC. In 2023 10th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON) 10(1),1321-1325. IEEE.

[4] Kotabagi, S., Sibandi, S. R., Nayak, R., & Patil, A. (2020). An 8 Bit Binary Weighted CMOS Current Steering DAC Using UMC 180nm Technology. In 2020 IEEE 17th India Council International Conference (INDICON) (1-5). IEEE.

[5] Patel, J. J., & Naik, A. P. (2020). Design and implementation of 4 bit binary weighted current steering DAC. International Journal of Electrical and Computer Engineering, IJECE, 10(6), 5642.

[6] Saud Almusallam, Ali Ashkanani, (2019). Differential Amplifier Using CMOS Technology.

[7] Uddin, N., Saha, P., Bhuyan, M. S. U., Iqbal, M. S., & Hossain, Q. D. (2022). Design and Analysis of Robust Two Stage Op-Amp using 90 nm CMOS Technology for Biomedical Applications. In 2022 International Conference on Recent Progresses in Science, Engineering and Technology (ICRPSET) (1-5). IEEE.

[8] Yadav, C., & Prasad, S. (2017). Low voltage low power sub-threshold operatioal amplifier in 180nm CMOS. In 2017 Third international conference on sensing, signal

processing and security (ICSSS) 35-38. IEEE.

[9] Kavyashree, C. L., Hemambika, M., Dharani, K., Naik, A. V., & Sunil, M. P. (2017). Design and implementation of two stage CMOS operational amplifier using 90nm technology. In 2017 International Conference on Inventive Systems and Control (ICISC), 1-4. IEEE.

[10] Tyagi, P., Bansal, K., Singh, S. K., & Praveen, P. (2021). Differential amplifier analysis on different technology nodes using Cadence Virtuoso. In Smart Computing (pp. 612-617). CRC Press.

[11] Soman, V., Mande, S. S., & Vijayakumar, K. (2023). A 4-Bit 4GS/s differential current steering DAC for 16-bit PAM transmitter in 45-nm CMOS technology. Applied Nanoscience, 13(3), 1959-1970.

[12] Tiwari, R. K., Mishra, G. R., & Misra, M. (2009). A new high performance CMOS differential amplifier. International Journal of Electronic Engineering Research, ISSN, 0975-6450.

[13] J Patel, J., & Naik, D. A. (2020). Comparative Study of Current steering DAC based on Implementation using various types of Switches. International Journal of Advanced Research in Engineering and Technology (IJARET), 11(4).

[14] Wen, M. K. K., binti Ahmad, N., bin Yusoff, Y., & Majid, H. A. (2021). Design of a 14-bit Hybrid DAC for High Resolution Applications in SAR ADCs. In 2021 6th IEEE International Conference on Recent Advances and Innovations in Engineering (ICRAIE) 6(1), 1-6. IEEE.

[15] Chakraborty, A., Joy, U. B., Dey, T. K., Hamim, Q. M. A., Chowdhury, S., & Hasan, M. (2023). Design of a Low-Power High-Gain Bulk-Driven Operational Transconductance Amplifier in 90 nm CMOS Process. In 2023 14th International Conference on Computing Communication and Networking Technologies (ICCCNT), 1-5. IEEE.

[16] Anbarasan, P., Hariharan, K., & Parameshwaran, R. (2016). Design of gain enhanced and power efficient Op-Amp for ADC/DAC and medical applications. Indian Journal of Science and Technology, 9(29).

[17] Vicuña, K., Mosquera, C., Rendón, M., Musello, A., Lanuzza, M., Prócel, L. M., ... & Trojman, L. (2021). A 180 nm Low-Cost Operational Amplifier for IoT Applications. In 2021 IEEE Fifth Ecuador Technical Chapters Meeting (ETCM) (pp. 1-6). IEEE.

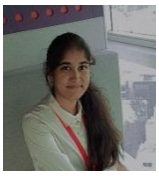
[18] Gupta, T., Bhandari, S., Taran, S., & Gupta, R. K. (2024). A 12-Bit 1.2-GS/s Current-Steering DAC in 45-NM CMOS Technology. Journal of Circuits, Systems and Computers, 2450256.

[19] Deveugele, J., & Steyaert, M. S. (2006). A 10-bit 250-MS/s binary-weighted current-steering DAC. *IEEE Journal of Solid-State Circuits*, *41*(2), 320-329.

AUTHORS

Jahnavi is a final year student at Chaitanya Bharathi Institute of Technology (CBIT), pursuing a Bachelor of Engineering in Electronics and Communication Engineering (ECE). With a deep interest in low power VLSI, digital electronics, and integrated chip design, Jahnavi is committed to pushing the boundaries of technology in these domains. Jahnavi's research focuses on developing innovative solutions to reduce power consumption in VLSI designs while maintaining high performance

Corresponding Author E-mail: jahnavieppala131@gmail.com



Geethamrutha is a final year student at Chaitanya Bharathi Institute of Technology (CBIT), pursuing a Bachelor of Engineering in Electronics and Communication Engineering (ECE). With a robust academic foundation and a keen interest in VLSI, embedded systems, and communications, Geethamrutha is dedicated to exploring cutting-edge technologies and their applications. Her areas of interest are low-power VLSI design, digital VLSI design. Geethamrutha's research focuses on enhancing the efficiency and performance of communication systems, leveraging their knowledge in both theoretical and practical aspects of electronics.
Email: geethamruthareddy@gmail.com

B.Khaleelu Rehman presently working as Associate professor in the Department of ECE, Chaitanya Bharathi Institute of Technology (Autonomous), Hyderabad, India. He received Ph.D. degree from University of Petroleum & Energy Studies, Dehradun and M. Tech from Jawaharlal Nehru Technological University, Hyderabad in VLSI System Design. He has 16 years of teaching experience out of which 8 years at the University of Petroleum & Energy studies, Dehradun. He had published research articles across globe viz. one SCI journal paper, 28 Scopus journal papers, 6 International conferences papers and authored two book chapters in world renowned publishers apart from possessing an Indian patent. He is a reviewer and editorial member for several reputed journals and also active member in several professional societies. He has conducted 10 workshops in the UPES and attended 21 workshops/short term courses/FDPs. He has been awarded Certificate of Appreciation from R & D Department, UPES during Academic years 2017-2018 and 2016-2017. He was the session chair for International Conference on Intelligent Communication, Control and Devices at Dehradun, India (Springer Conference) viz. ICICCD-2016, ICICCD-2017 and ICICCD-2018. He was invited to give guest lectures at various places in India on innovative topics. He is a senior member in IEEE Circuits and systems Society. His area of interest includes Digital

Signal processing, VLSI Design, Digital VLSI Architectures and Analog Circuits.

E-mail:Khaleelurehmanb_ece@cbit.ac.in

E. Chandrasekhar is working as Assistant Professor in the department of Electronics and Communication Engineering, CBIT (A) . He is pursuing his Ph.D. from JNTU-K in the area of VLSI; he did his M.E (Embedded Systems &VLSI Design) form University College of Engineering, O.U and he did his B.Tech (ECE) form GATES Institute of Technology, JNTU. His research interest includes Analog and mixed signal IC Design. He has 14 years of experience in teaching. He has published over 15 research papers in International Journals and Conferences.

E-mail: echandrasekhar_ece@cbit.ac.in

P. Chandra Sekhar received the B.E. degree in and Communications Engineering from Sir. C. R. R College of Engineering (A. U) in 2003 and M. Tech in Electronics from B.M.S College of Engineering – Bangalore (V.T.U) in 2009 and pursing Ph.D. in Electronics and Communication Engineering from JNTU-Kakinada. He is working in the area of VLSI and "Communication and Signal Processing". He is author of several IEEE conference papers and Journals. The flowing text books "VLSI Design" and "5G and IoT" are under his credential. He is presently working as an Assistant Professor in the department of ECE, CBIT(A) – Hyderabad.

E-mail: pchandrasekhar_ece@cbit.ac.in