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Design and Implementation of BIST Architecture for Static Parameter of ADC

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ABSTRACT:

This paper provides a comprehensive analysis of On-Chip ADC BIST and compare it to the Off-Chip static parameter, which is the non-linearity of SAR ADC. It also evaluates the parameter i.e, INL, DNL offline using raw data names off-chip method which required some offline calculation to characterize the BIST circuit. whereas on-chip method does not require this kind of extra calculation in this method parameter evaluate in background and lock the pass/fail status in memory location. To demonstrate sufficient test accuracy also includes both calibrated and uncalibrated data for ADC. An algorithm known as USER-SMILE (ultra-fast segmented stimulus error identification algorithm) that is adopted in hardware unit to calibrate ADC, the solution has been tested for 12-bit SAR ADC in test vehicle project as well as General purpose project of 28nm automotive microcontroller. This solution enables the faster execution time and reduce tester time.

KEYWORDS

R2R DAC, SAR ADC, BIST, static linearity testing, DNL, USERSMILE algorithm unit, USMILE Algorithm unit

1. INTRODUCTION

ADCs i.e., analog to digital converters are majorly used IP in Analog to digital converters (ADCs) in analog and mixed signal devices. Now a days testing of an ADC, especially for high resolution, is very difficult. As manufacturing cost falls, testing costs increase dominate overall costs. The main reason why ADC testing costs so much is because of the time it takes to run the test. To test the non-linearity of ADC, earlier used histogram method that is dependent on very linear signal and there should not be any missing code. The linear signal is generated by high precision automated test equipment. So, the source should be more precise and should have more linearity than the device under test like ADC or DAC.

Now a days semiconductor industry is using the High speed and high-resolution ADCs that add some drawback in histogram testing method as it requires more samples than number of transitions in the ADC means sampling rate is require high.

To complete the histogram test method, it requires more samples for high resolution ADC, which adds time and expense to the test process. Certain methods of linearity testing merely examine a smaller number of codes to manage testing costs. The non-stationary of the test extended test duration. Additionally, it becomes problematic when resolution of ADC increases then a highly linear source will be not always precise or stationary as it requires.

A challenge in AMS testing is meeting strict requirements for the linearity of the input signal over a very long test time. Many techniques have been developed recently by researchers to meet the input signal's strict requirement, which is the result of significant work done to address these challenges.

However, because of the high resolution or speed of ADC, designing such a signal generator is not simple. The costs are frequently higher when the design is more complex. On the other hand, some researchers have created an algorithm that lowers the requirements for stimulus linearity. The SIER (Stimulus error identification and elimination) algorithm is suggested as a means of employing nonlinear stimuli to assess the accuracy of ADC. The offset should be constant when identifying the nonlinearity error of signal source. For ADC full code INL/DNL testing, the built-in-self test becomes useful when input signal linearity requirements are loosened. But SEIR relies on histogram approach, which necessaries a lengthy testing period. For ADC test, test time is also very important. Numerous strategies to shorten test time have been put forth. The algorithm known as USMILE (ultra-fast segmented model linearity error identification) was introduced in modelling the ADC's INL require a radically different strategy.

To test the ADC, generally an external instrument needs to ramp the input and signal the waveform, but in this solution the BIST solution, the ADC receives the input from the R2R ladder DAC. Instead of requiring a separate signal generator, on-chip resources can be used for data

processing. This means that parameter testing devices are not required. This saves costs for external testing devices. The on-chip ramp is generated using a 14-bit DAC.

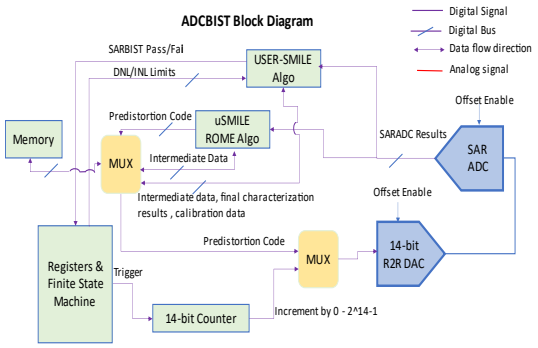


Fig. 1: ADC BIST Block Diagram

There are many algorithms for eliminating linearity errors. SIER: Stimulus error detection and elimination and the USER-SMILE algorithm are more popular. But it's neither easy nor practical to build a very simple signal generator on a chip because it costs more and doesn't work as well. This solution proposed the USERS-SMILE algorithm instead of the SIER method because it requires a long testing time. In this method we use two signals that are not straight lines and have a different constant voltage.

2. ADC BIST SUBSYSTEM BLOCK

This block is made up of several components, including SAR ADC, a R2R ladder DAC, a finite state machine (FSM), a USER-SMILe algorithm that is in form of hardware unit, a small size storage memory to store DAC code and other data, also contain a MUX unit to select the test mode or normal mode.

The finite state machine, also known as FSM, is a small part used to identify and remember patterns. A group of registers is used to hold pattern. In simpler terms, it manages the order in which the different parts of BIST system work together.

Initially we turn ON the BIST with test mode selection, after that FSM turn ON 14-bit counter that must send control word to DAC. When there are significant changes in the ADC, the USER-SMILE calculation unit for post handling begins working. This process will continue till it has been covered all control word and a substantial BIST pass/fail status has been given. MUX unit is a subcomponent that helps the BIST block take control over the DAC and ADC by bypassing their usual routes for control and data. The algorithm unit is a solid version of the USER-SMILE algorithm. It consists of a small memory unit that is used to store data and code. We may utilize a portion of framework within the Soc to form the arrangement littler.

2.1 12 -BIT SAR ADC

The ADC being tested is a type of analog-to digital converter that uses a method called charge redistribution. It is a single-ended ADC, meaning it measures the voltage of one signal at a time. To make sure the ADC BIST solution is working correctly, nonlinearity is tested for both methods using Histogram Ramp test. This test is used to compare and check the accuracy of the results.

If we use off-chip test methodology for ADC test, then must generate ramp signal by using external device but that should be accurate. So, avoid this method an on chip R2RDAC is used to generate ramp signal for BIST testing that is more accurate then off-chip method. After then a histogram test method used to calculate non-linearity in terms of differential non-linearity/integral non-linearity, offset and gain error.

The optimal straight-line method is typically chosen because has better non-linearity results. INL is calculated using the best fit line method. The measurement of INL specification, which can be explained as follows, occurs after the gain and static offset errors are eliminated.:

$$INL = \sum_{n=0}^{2^N-1} \text{DNL}$$

Where: n=DAC Code that varies from 0-2^N-1 and resolution of ADC is denoted by N.

INL can be calculated as summation of DNL also in another way-

$$\text{INL} = Ck - Cideal/1LSB$$

Where, Ck and Cideal denote actual and ideal transition from k-1 to k code respectively. And 1LSB is ideal step size that calculated as (1LSB= VFSR/2^N), VFSR is full scale range for input supply voltage and N is again resolution of ADC. of ADC and the transition is exactly 1LSB apart.

Another type of static error that is defined for ADC is DNL i.e., differential nonlinearity that define as difference between ideal and actual analog value expressed in LSB. an ADC transfer function that does not have any missing code or if ADC samples each code without missing any one then that system has DNL error less than or equal to 1LSB. When the

ADC's digital output rises in response to an increasing input signal, then the transfer curve's slope has remained constant so gain and offset error are eliminated.

DNL error is defined as

DNL=|Ck+1-Ck)/1LSB]-1|; where 0 < k < 2^N-1.

Ck is the analog value corresponding to the digital output code, N is the number of bits for ADC resolution.

2.2 R2R DAC

High-definition television, mobile phones, and audio all use digital-to-analog converters (DACs). DAC is the mostly used device with ADC in analog and mixed signal devices. The car microcontroller has a part called 14-bit DAC, which is made in robust ladder design. Corresponds to what is necessary. BIST has a test mode and a control mode. There is a built-in counter that generates the code 0 to 2^N-1. When test mode is activated, the counter begins counting and the DAC begins receiving information code from the counter.

The DAC is now started to send input to ADC, and the ADC samples the output and measure the nonlinearity after sampling DAC codes. There is no need to test the DAC for accuracy as it is heavily tied to the USER SMILE algorithm unit.

A system on chip (SoC) is integrated into DAC testing, which involves measuring the gain error and integral and differential nonlinearities (DNL and INL). In this solution, the USE SMILE algorithm is used to perform the static linearity tests of the DAC, instead of the conventional methods of using a digital waveform recorder or digital voltmeter.

2.3 uSMILE ROME Algorithm Unit-

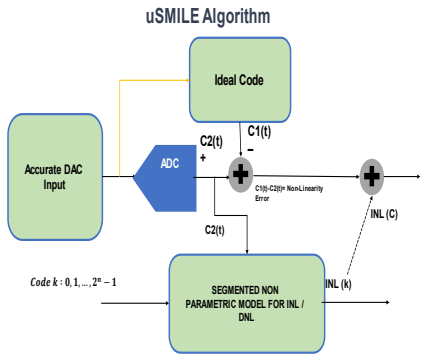


Fig 2: uSMILE Rome algorithm block

In order to attain greater accuracy and drastically cut down on testing time, the uSMILE algorithm was suggested. With significantly less test data, the algorithm can capture ADC nonlinearity using a segmented nonparametric model and system identification approach.

The INL curve's segmented non-parametric model divides the INL into various segments. There is an error term that corresponds to each segment. MSB error define as $e_M(C^1{}_{MSB})$where $C^1{}_{MSB}$is the code of the MSB bits. Like this "segmented INL" refer to the definitions of $e_I\left(C^{(1)}{}_{ISB}\right), e_L(C^1{}_{LSB})$ for ISB and LSB errors respectively. (The following will be code C's final INL value.

$$\text{INL(C)}=e_M\left(C^{(1)}{}_{MSB}\right)+e_I\left(C^{(1)}{}_{ISB}\right).+e_L\left(C^{(1)}{}_{MSB}\right).$$

It is vital to produce the digital stimulus and record the analog response to test the linearity of a DAC. For a conventional testing method, a digital voltmeter (DVM) is used to measure the output voltage at each, which records the DAC's input code from zero to maximum level in terms of analog voltage. Averaging of samples is done to get minimum noise error. Calculating INL and DNL involves comparing these voltages to ideal voltage anticipated for each code.

There are two ways in which this occurs. Initially, the algorithm capitalizes on the fact that there are comparatively fewer truly independent sources of error than DAC codes that require linearity testing. As a result, it will reduce the testing time as it takes few samples to perform linearity test than actual or typical sample. Secondly it measures the DAC's output signal using the integrated digitizer rather than using a conventional high-precision digital voltmeter. As a result, testing times between samples are shortened. Testing expenses are subsequently decreased as a direct result of this testing time reduction.

2.4 USER-SMILE ALGORITHM UNIT:

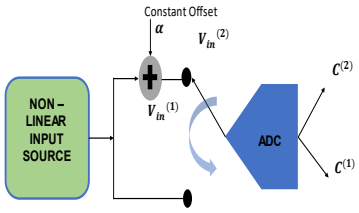


Fig 3: USER SMILE algorithm block

Where:

$\alpha = constant\ voltage$
$w = input\ -referred\ noise$
$q = quantization\ noise$
$e_M = MSB\ segment\ avg.\ error$
$e_I = ISB\ segment\ avg.\ error$
$e_L = LSB\ segment\ avg.\ error$

The INL has been divided in three segments MSB, ISSB and LSB. Equation - can be used to express the total nonlinearity error for code C in the same format.

$$V_{in}^{(1)} + w^{(1)} = C^{(1)}.V_{LSB} + e_M\left(C^{(1)}{}_{MSB}\right).V_{LSB} + e_I\left(C^{(1)}{}_{ISB}\right).V_{LSB} + e_L\left(C^{(1)}{}_{MSB}\right).V_{LSB} + q^{(1)}$$

$$V_{in}^{(2)} + w^{(2)} = C^{(2)}.V_{LSB} + e_M\left(C^{(2)}{}_{MSB}\right).V_{LSB} + e_I\left(C^{(2)}{}_{ISB}\right).V_{LSB} + e_L\left(C^{(2)}{}_{MSB}\right).V_{LSB} + q^{(2)}$$

$$C^{(1)} - C^{(2)} - \frac{\alpha}{V_{LSB}} = -e_M\left(C^{(1)}{}_{MSB}\right) - e_I\left(C^{(1)}{}_{ISB}\right) - e_L\left(C^{(1)}{}_{MSB}\right) + e_M\left(C^{(2)}{}_{MSB}\right) + e_I\left(C^{(2)}{}_{ISB}\right) + e_L\left(C^{(2)}{}_{MSB}\right) + \frac{\left(q^{(2)} - q^{(1)} + w^{(1)} - w^{(2)}\right)}{V_{LSB}}$$

An expedient method for addressing error during testing is called ultrafast stimulus error removal. While they can only correct specific types of error and don't shorten the time required for data collection, existing methods like the histogram based SIER method have certain drawbacks. The smallest possible integral non-linearity (INL) is the aim of ADC static linearity. Correct adjustment to ADC static linearity is made possible by full-code information regarding INL. The results of the BIST solution should be used to fix linearity errors in the ADC since it contains all the information regarding INL.

This technique uses two non-aligned input signals with a fixed offset in between. After then, ADC receives these. The final INL could be shown using a partial non-parametric demonstration. We determine the INL of ADC indirectly by subtracting the two sets of output code, as opposed to directly. Compared to the suggested histogram approach, the test's accuracy and scope are far higher.

2.5 FEATURES OF USER-SMILE ALGORITHM UNIT

This unit can be used as hardware as well as software option. as this unit used in microcontroller and this system was on chip so it could be evaluated as software option, but it has been observed that software approach is costly then hardware approach. So, for this solution it's been used this algorithm as hardware unit.

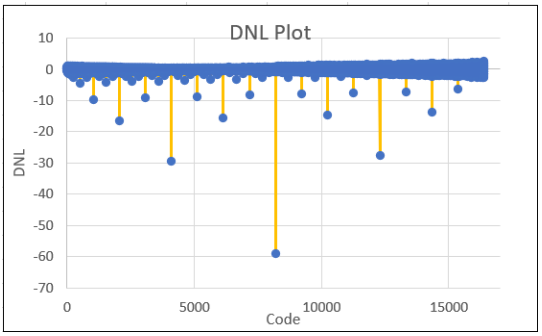
Also, if we use hardware unit then it's removed dependency on on-chip processor. Rather processor is available or not then also we can test the ADC parameter without affecting system. This feature makes it usable for test vehicle projects, where an IP is tested individually without connecting with processor. Also, if the on-chip processor is busy handling another task then also won't be critical.

It can save memory space also. as software algorithm implementation required memory either RAM or ROM to store its program, but hardware unit does not require the memory so free memory can be utilize for other application. In short no system memory is required for this implementation although small memory is used to hold ADC code that is used static RAM memory.

It will reduce the execution time as hardware approach speeds up the execution time. This will help to reduce power on self-test execution time. In other words, the hardware approach has many advantages over the software approach.

3. BIST TEST RESULT

Data shown without BIST Calibration. Which has high INL/DNL value but still fall under the specs. In On chip BIST solution max values for DNL and INL is locked in specified memory location with pass and fail status of SARBIST using USER-SMILE algorithm unit and there is no need to plot each data point. If user want to check the data point, then fetch from memory location and INL/DNL graph can be plotted.



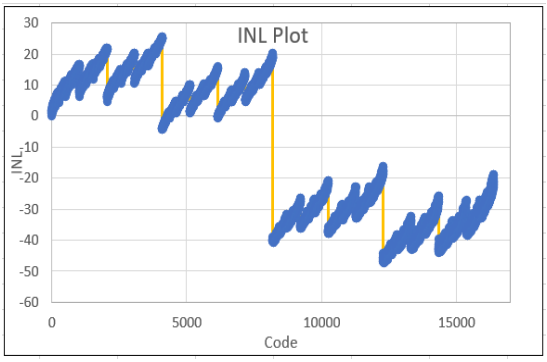


Fig 4: Uncalibrated DNL/INL Plot

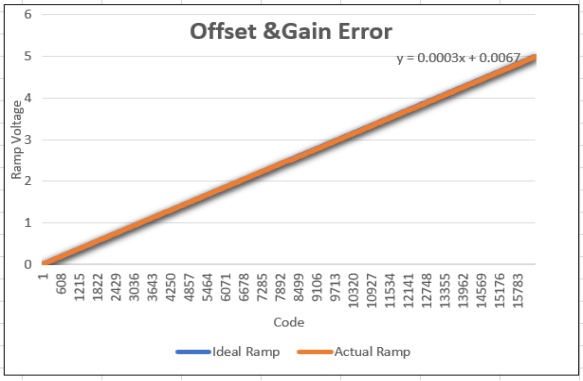


Fig 5: Offset and Gain error.

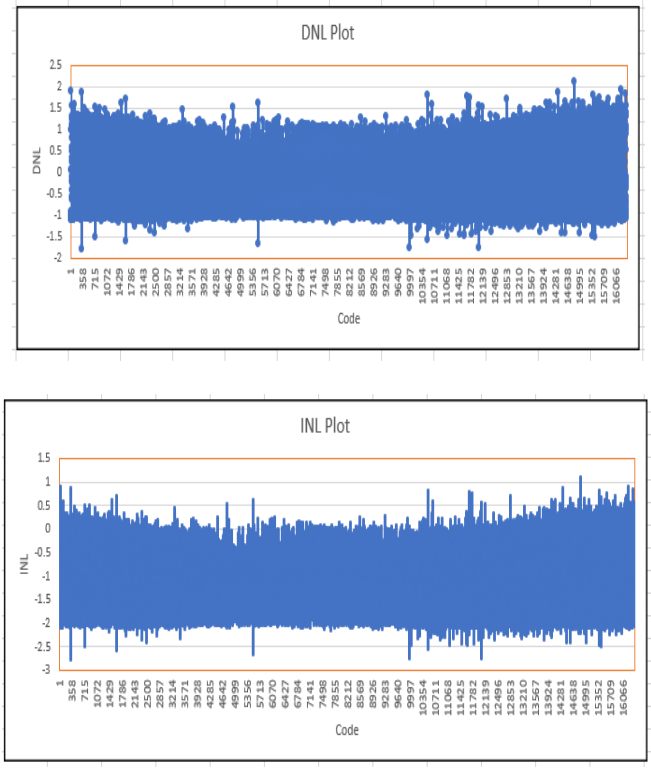


Fig 6: Calibrated Off chip INL/DNL Plot

To check if the ADC BIST solution is trustworthy, data has been plotted for comparison between on chip and Off chip method where Off chip calibration done using code alienation method. In which 0-16383 code captured and removed offset by comparing with ideal codes. On chip calibration has been done using uSMILE ROME algorithm and calibration code generated names as predistortion code. Both On chip and Off chip data is following same trend also fall under predefined the limits for INL and DNL. Offset and Gain error also calculated and plotted for ADCBIST subsystem. When the transfer function deviated from the actual staircase response then offset error is calculated. The gain error specifies the deviation of the last transition from the ideal.

The complete BIST solution takes up a space of 40nm CMOS technology. There are specific limits that have already been established. The results obtained are compared to these limits. Depending on the comparison, a pass or fail status is shown.

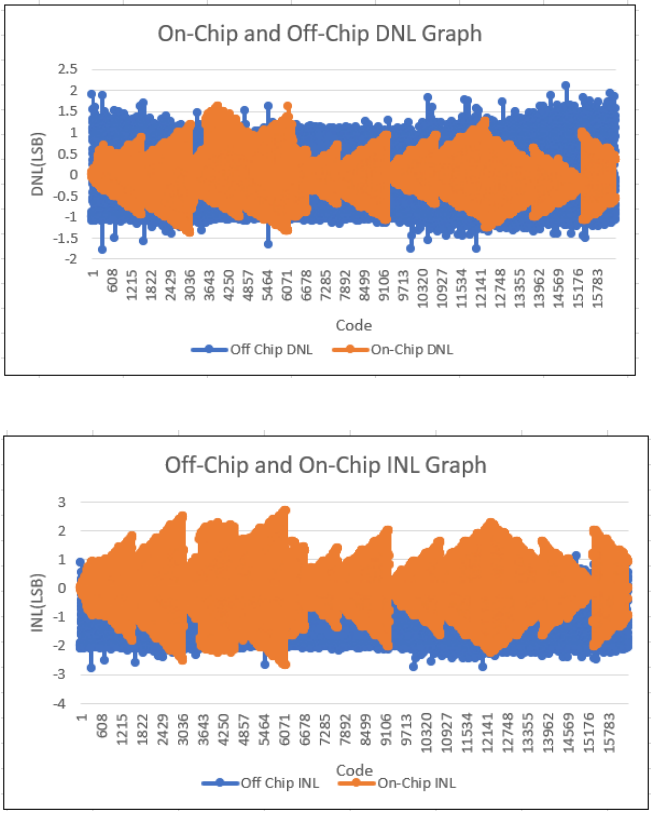


Fig 7: Calibrated DNL/INL Correlation

4. CONCLUSION

A plan for testing an ADC has been shown and examined. It gets rid of the need for a good external test machine and makes testing much quicker. They have done a part of investigation to appear how well the BIST arrangement works. The procedure is used to calibrate an ADC to get precise

output and execution in both inactive and changing conditions. This allows testing of the performance of in field ADC, which is needed to meet strict safety requirement in specific a application, self-driving cars. BIST circuit's physical space is so small, so money saved from testing.

5. ACKNOWLEDGEMENT

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