ISSN: 2584-0495 Vol. 2, Issue 10, pp. 1269-1275

International Journal of Microsystems and IoT

ISSN: (Online) Journal homepage: https://www.ijmit.org

Thickness Dependency Analysis of IGZO-Based Thin Film Transistor

Akshay Verma, Nitesh Kashyap

Cite as: Verma, A., & Kashyap, N. (2024). Thickness Dependency Analysis of IGZO-Based Thin Film Transistor. International Journal of Microsystems and IoT, 2(10), 1269-1275. https://doi.org/10.5281/zenodo.14168632

Published online: 30 October 2024

DOI: https://doi.org/10.5281/zenodo.14168632

International Journal of Microsystems and IoT
Vol. 2, Issue 10, pp.1269-1275; DOI: https://doi.org/10.5281/zenodo.14168632

Thickness Dependency Analysis of IGZO-Based Thin Film Transistor

Akshay Verma, Nitesh Kashyap

[1]Department of Electronics and Communication Engineering, Dr B R Ambedkar National Institute of Technology, Jalandhar

ABSTRACT
This paper highlights the thin film transistors used in the latest applications and devices. The working principle of thin film transistors with various device structures can be used to fabricate thin film transistors. Progress in the latest materials that are being used in applications like LCDs, sensors, RFID tags, Displays, etc. The remarkable characteristics of Indium-Gallium-Zinc Oxide (IGZO) thin films, for instance, their transparency and high mobility, have generated significant interest in the application part of Thin-Film Transistors (TFTs). The operation of a-IGZO TFTs taking four different insulators [Si_3N_4, SiO_2, HfO_2, and Al_2O_3] into consideration by varying insulator thicknesses is studied by simulating it over Silvaco [Atlas] TCAD Tool.

KEYWORDS
TFT; amorphous-IGZO; Insulator; Simulation; MOSFET; AMOLED; OLED

1. INTRODUCTION

Thin-film transistors abbreviated as TFTs, are a form of transistor technology that is widely utilized in Liquid Crystal Displays (LCDs) and Organic Light-Emitting Diodes (OLEDs). Over the past several years, OLED screens have become increasingly popular, especially for usage in mobile apps. Reducing the power usage of these displays is essential due to the restricted life of the battery. Reducing the refresh rate of the pixel circuit is one possible way to minimize the power being consumed. [1,2]

When compared to well-recognized transparent oxide semiconductors (TOS); the indium oxide (In_2O_3), indium-doped zinc oxide (IZO), zinc oxide (ZnO), and transparent amorphous oxide semiconductors (TAOS) got more attention. [3,4]

Enhancing these displays' performance and image quality is mostly due to TFT technology. TFTs are fundamentally a Field-effect transistor (FET) type, in which gate electrodes are used to alter electric fields to modulate the current at the deposited semiconducting thin film. In this case, a gate-bottom TFT made more sense to me.

As seen in the Bottom-down TFT's schematic view, there is a Drain, a Source, and Channel Material like a-Si. Poly-Si, Organic Semiconductors, Oxide Semiconductor, Gate Dielectric like SiO_2, and Al_2O_3 and Gate Electrodes on Substrate Glass TFT are mostly used as pixel addressing elements and as driving transistors in active-matrix organic light-emitting displays (AMOLEDs) and active-matrix liquid crystal displays (AMLCDs). An amorphous indium-gallium-zinc oxide (a-IGZO) being the most favorable TAOS has several advantages, including greater mobility, a wider band gap, improved transparency, and room temperature deposition. There are many uses for amorphous-IGZO, particularly in TFTs. Conventional TFTs depending on zinc oxide (ZnO), organic semiconductors (OSC), or amorphous silicon (a-Si), were superseded by TFTs based on a-IGZO.

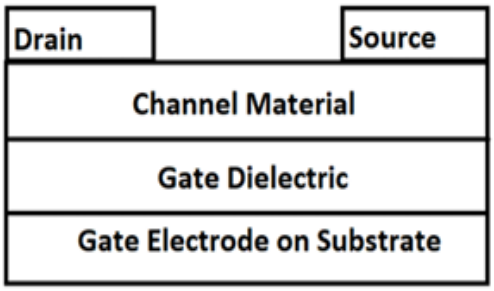

Fig. 1; Schematic view of Bottom-Down TFT

For usage in TFTs, a variety of gate insulators have been researched, which includes Silicon Nitride (Si_3N_4) [12,13], Silicon Dioxide (SiO_2) [11], Hafnium Oxide (HfO_2) [14,15], Aluminium Oxide (Al_2O_3) [16,17].

It is crucial to remember that TFTs are a particular kind of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), that is made by covering an insulating substrate with a dielectric layer, a metallic connection, and an active semiconductor layer.

Novel materials with excellent mobility and cheap production costs are becoming more and more relevant as the need for intelligent and flexible electronic devices and integrated systems increases. One important use for printed electronics is printable TFTs. Materials with channel semiconducting properties affect printed TFT performance. Additionally, some factors are critical to TFTs, including mobility, threshold voltage (V_{th}), subthreshold slope and I_{on} to I_{off} ratio. The figure illustrates the general procedure for creating metal oxide semiconductor thin films and related TFT devices using solution methods.

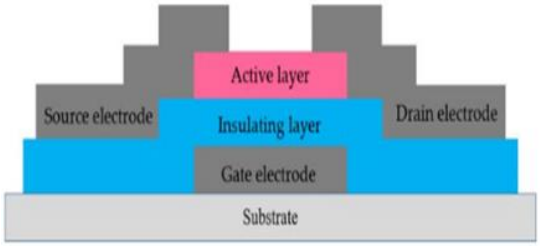

Fig.2; Schematic Diagram of TFT Device

A particularly strong tool for studying and simulating electronic devices is TCAD from SILVACO software, which is used for numerical simulation. Several parameters that model the phenomena observed in experiments can be varied with TCAD. The influence of insulators is explained numerically independently of the contribution of other parameters like the constant charge in insulator material or the states of interface in between the insulator and the semiconductor material. In experiments, these separations are not possible to achieve. Moreover, numerical simulation reduces the expense and measuring duration. This is also evident that an exhaustive investigation of insulators and effects due to instability are exceedingly challenging through experimentation.

2. DEVICE STRUCTURE AND SIMULATION PARAMETER

In this section, the 2-D structure of the proposed IGZO-based thin film transistor (TFT) has been described which is shown in Fig: 3 which shows a 2-D schematic representation of a-IGZO TFT structure used in this paper, with insulator material of SiO_2. We are considering this for reference along with the parameters and dimensions which we will simulate by varying parameters.

The insulator layer thickness distinguishes the four types. Al_2O_3, HfO_2, SiO_2, and Si_3N_4 are the four types of insulators. Fig. 3 depicts the architectural representation of a-IGZO TFT structure that was examined in this paper.

Fig: 3; Two-dimensional schematic representation of amorphous-IGZO TFTs structure used in this paper

It comprises a 20 µm thick amorphous-IGZO active channel, a 100 µm thick layer of insulator, and a substrate of a polycrystalline silicon wafer (n^{++}) that serves as gate to the device. The dimensions of the channel are 30 µm in length and 180 µm in breadth. Titanium (Ti) is used to make the 5 µm thick source and drain.

This work employed numerical simulation to observe the outcome of thickness variation of insulator genre on a-IGZO TFT performance. We compare and contrast the insulators SiO_2, Si_3N_4, Al_2O_3, and HfO_2.

3. PHYSICAL MODEL

The Poisson which is a non-linear system and Continuity equation is best solved numerically to provide information about the effects of several technological and physical parameters involved in the operation of the device. The electronic events inside the associated electrical transport mechanism and semiconductor are described by the Continuity and Poisson's equations, which are useful techniques for understanding the physics of materials and embedded electronic devices. Additionally, this is an inexpensive and important tool to improve the architecture and operation of semiconductor devices.

It is well known that the narrow acceptor tail state g^{A}_{ct} (E), which is located around EC, the state of donor tail g^{D}_{vt} (E), which decays exponentially against the EV. In contrast, the Gaussian distribution of donor g^{D}_{G} (E), which is maximized at 2.9 eV (from EV) at a width of 0.1 eV, together form the amorphous-IGZO density of gap states. The expression for these distributions is as follows: [5,6,7,8]

$$g^{D}_{v_t}(E) = N_{td}\, X\, ex\,\mathrm{p}\left(Ev - \frac{E}{Wtd}\right) \quad (1)$$

$$g^{D}_{G}(E) = N_{gt} X \exp\left(-\frac{(E-egd)2}{Wgd}\right) \quad (2)$$

$$g^{A}_{Ct}(E) = N_{t_a}\, X \exp\left(E - \frac{Ec}{Wta}\right) \quad (3)$$

Poisson's equation, which connects the density of space charge to the electrostatic potential and can be written in mathematical form as,[10]

$$div(\varepsilon\nabla\Psi) = -p = -q\,(p - n + \mathrm{n_{tail}} - \mathrm{p_{tail}} + n_{g_d} - P_{ga} + N_d) \quad (4)$$

where; N_d - Doping concentration of n-channel,
p - Local density of space,
p_{tail}, n_{tail}, n_{gd} - The charge states of the band gap,
Ψ - Electrostatic potential, ε - Local permittivity, and n and p - Densities of the free carriers.

In the dynamic mode, the equations of continuity for holes and electrons are given as [10]

$$\frac{\partial n}{\partial t} = \frac{1}{q}\, div\, \overrightarrow{J_n} + G_n - R_n \quad (5)$$

$$\frac{\partial \rho}{\partial t} = -\frac{1}{q}\, div\, \overrightarrow{J_p} + G_p - R_p \quad (6)$$

In steady state, $\frac{\partial n}{\partial_t} = \frac{\partial \rho}{\partial t} = 0$

$\vec{J}_\rho$ and $\overrightarrow{J_n}$ represents the hole and electron current densities, and the generation rates for holes and electrons, G_n and G_p, are disregarded in current work. The electron charge is q, and the recombination of the total rate of holes and electrons in the tail and Gaussian states are Rp and Rn. The current densities in the drift-diffusion model are given by the quasi-Fermi level n and p, respectively, as follows:

$$\overrightarrow{J_n} = -q\mu_n n \nabla \phi_n \quad (7)$$

$$\overrightarrow{J_p} = -q\mu_\rho \rho \nabla \phi_\rho \quad (8)$$

where the electron and hole mobilities are denoted by n and p, respectively.

The carrier concentration and potential are connected to the quasi-Fermi levels via

$$n = n_i \exp\left(\frac{\psi - \phi_n}{k_B T}\right) \text{ and}$$

$$\rho = n_i \cdot \exp\left(\frac{\psi - \phi_\rho}{k_B T}\right)$$

where n_i represents intrinsic concentration at absolute temperature, T.

Physical parameters are applied to the equation of continuity. The second one is resolved for various applied gate voltages within -10V to 20V range. The transfer characteristics (I_D v/s V_{GS}) are displayed on a semi-logarithmic-scale, at a fixed drain voltage of 0.1V.

4. RESULT & DISCUSSION

Using the information in Table 1, TCAD solves the Poisson's and Continuity Equations to determine how the insulator affects the procedure of amorphous-IGZO TFTs. In this case, the gate voltage applied varies between -10V to 20V for a V_{ds} of 0.1V. Fig. 5 displays the transfer characteristics (I_{DS} v/s V_{GS}) on a linear and semi-logarithmic scale. Using regular equation for a MOSFET, which is provided by: [9]

$$I_d = \mu_{e_{ff}} C_{ox} \frac{w}{L} \left(v_{g_s} - v_{\text{th}}\right) \cdot v_{d_s}$$

where;

L and W indicate the length and width of the TFT channel, respectively,

I_d is channel current,
V_{gs} indicates voltage at the gate electrode,
V_{ds} indicate the voltage at the drain electrode,
C_{ox} indicates the dielectric capacitance per unit area.

Table 1
The physical characteristics of various a-IGZO TFT layers utilized in this paper [18,19,20]

Layer	Parameter	Designation	Value
SiO_2	E_g (eV)	Energy	9.0
	K	Dielectric constant	3.90
	T (μm)	Thickness (μm)	10
			30
			50
			70
Si_3N_4	E_g (eV)	Energy	5.3
	K	Dielectric constant	7.5
	T (μm)	Thickness (μm)	10
			30
			50
			70
Al_2O_3	E_g (eV)	Energy	8.8
	K	Dielectric constant	9.3
	T (μm)	Thickness (μm)	10
			30
			50
			70
HfO_2	E_g (eV)	Energy	6
	k	Dielectric constant	22
	T (μm)	Thickness (μm)	10
			30
			50
			70

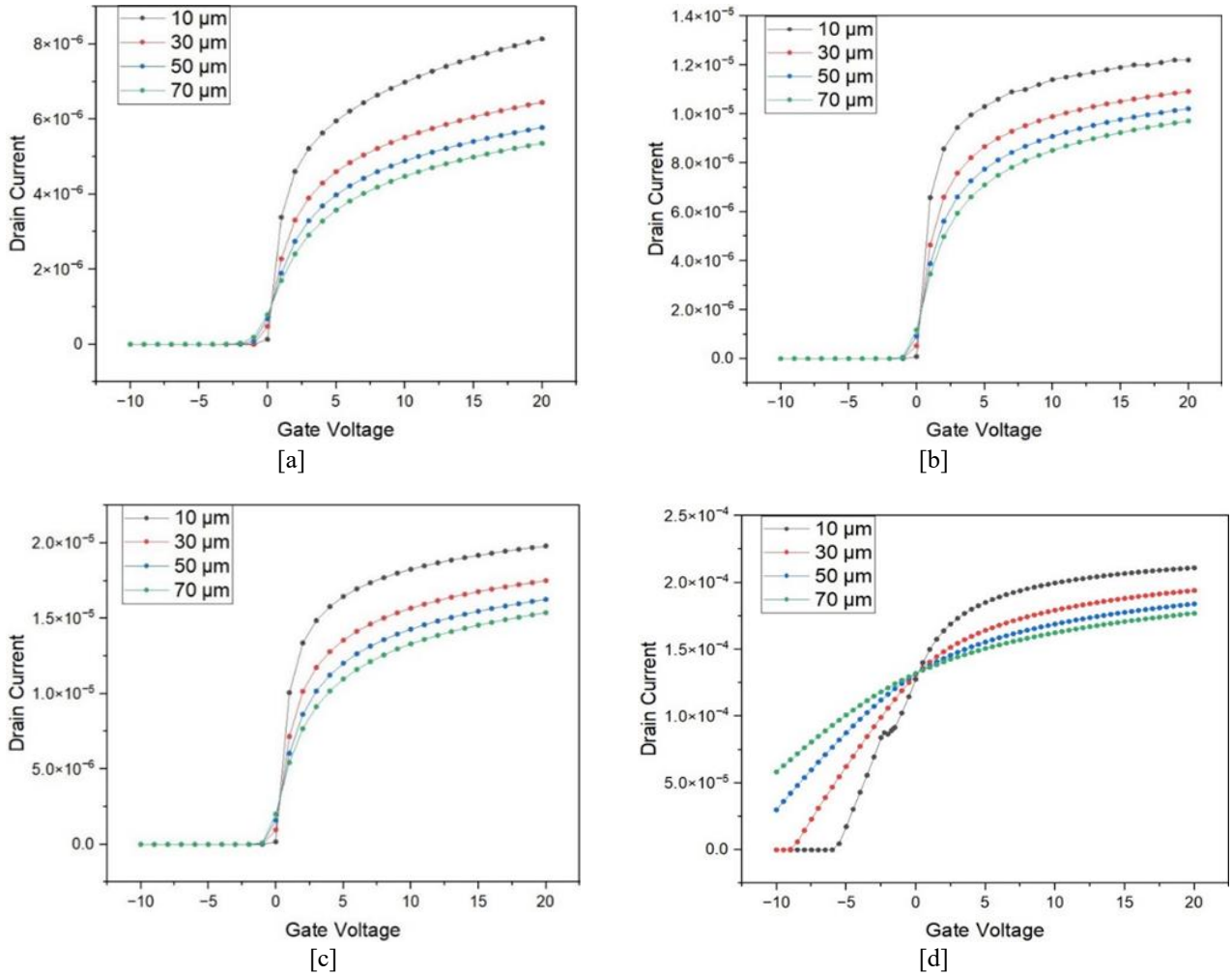

Fig: 4 The transfer characteristics for different dielectric thicknesses of [a] SiO_2, [b] Si_3N_4, [c] HfO_2, [d] Al_2O_3

The above results represent the transfer characteristics of four different insulator materials SiO_2, Si_3N_4, Al_2O_3, and HfO_2 having four different thickness levels each as 10 µm, 30 µm, 50 µm, and 70 µm, respectively. The physical characteristics of amorphous-IGZO TFT layers i.e., SiO_2, Si_3N_4, Al_2O_3, HfO_2 are mentioned in Table 1.

Fig 4 (a) indicates the transfer characteristics of SiO_2 insulator material. Fig 4 (b) indicates the transfer characteristics of Si_3N_4 insulator material. Fig 4 (c) indicates the transfer characteristics of Al_2O_3 insulator material. Fig 4 (d) indicates the transfer characteristics of HfO_2 insulator material. It is noted that when the thickness of any of the four insulator materials is decreased from its reference thickness of 100 µm, the transfer characteristics that result are better than those at higher or earlier thicknesses. The drain current increases with decreasing insulator material thickness. This indicates that for all insulator materials, the thickness characteristics obtained at 10 µm are superior to those obtained at 30 µm, 30 µm is superior to those obtained at 50 µm, 50 µm is superior to those obtained at 70 µm, and 70 µm is superior to those obtained at 100 µm, which is the reference thickness.

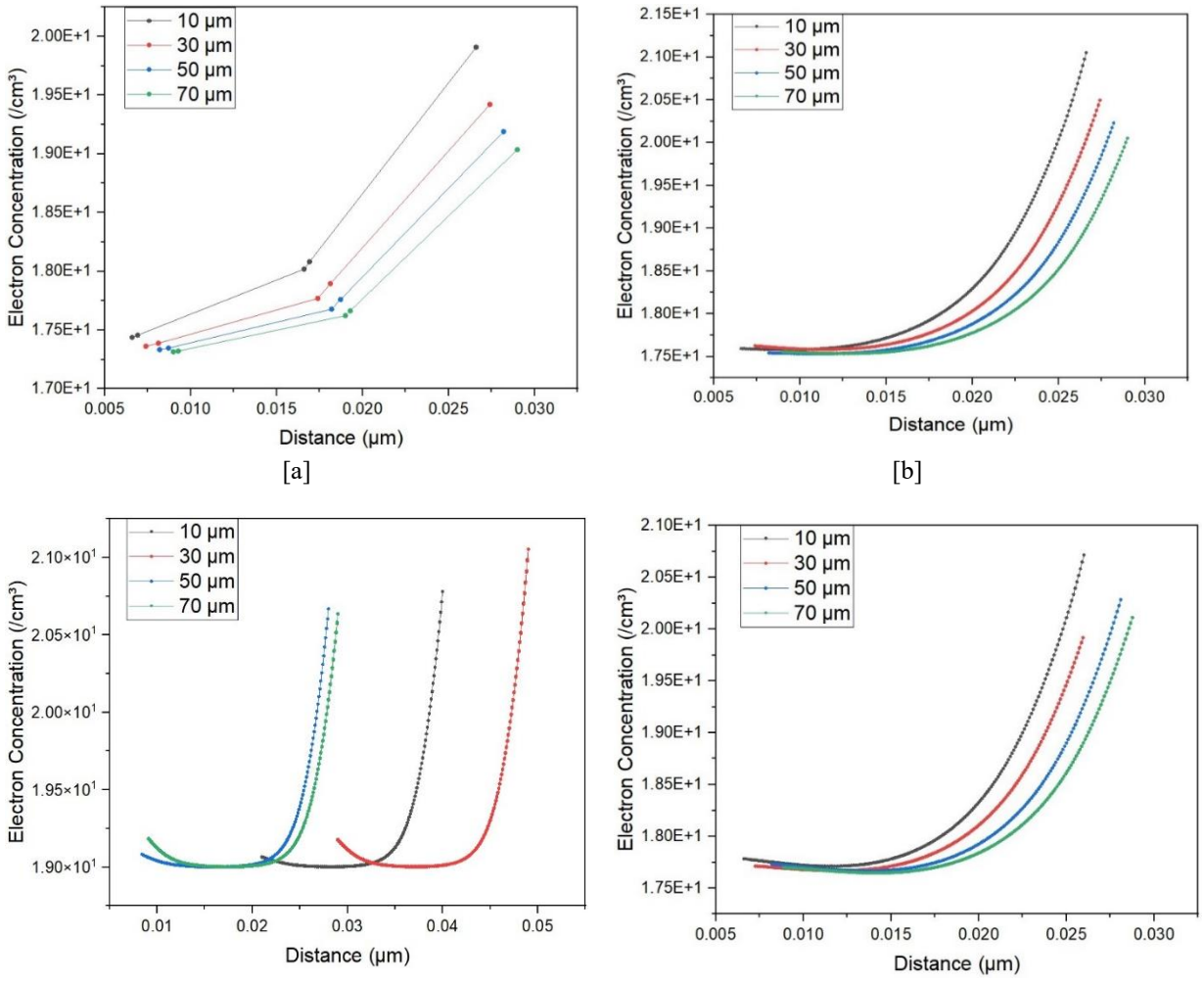

Fig: 5 [a] represent the electron concentration for different thicknesses of SiO_2, [b] represents the electron concentration for different thicknesses of Si_3N_4, [c] represents the electron concentration for different thicknesses of HfO_2, [d] represents the electron concentration for different thicknesses of Al_2O_3, and $V_{DS} = 0.1V$

It is found that the ε_{ox} (relative permittivity) determines the insulator-class influence on the performance of the TFT. The TFT performance is improved at higher relative permittivity values. Internal factors like the electric field and electron concentration are retrieved to comprehend this influence. Figures 4 and 5 display the transfer characteristics and electron concentration, respectively. The electron concentration for various SiO_2, Si_4N_4, Al_2O_3, and HfO_2 thicknesses is depicted in Figure 4.

5. CONCLUSION

Using numerical modeling, the stability and performance of the gate dielectrics have been examined and analysed for a-IGZO TFTs having insulated materials SiO_2, Si_3N_4, Al_2O_3, and HfO_2. The outcomes of the simulation demonstrate the improved performance that was attained. The HfO_2 insulator demonstrated a high level of stability compared to SiO_2, Si_3N_4, and Al_2O_3. However, the instability of a-IGZO was shown to be unaffected by the kind of gate insulator. As the donor Gaussian density of states increases, the gate insulators SiO_2, Si_3N_4, Al_2O_3, and HfO_2 exhibit deterioration. In oxide TFTs, a well-chosen gate dielectric can improve device durability. Consequently, decreasing the instability will benefit from improving the materials used in gate dielectrics.

REFERENCES

1. Nomura, K., Ohta, H., Takagi, A., Kamiya, T., Hirano, M., Hosono, H. (2004). Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. Nature 432, 488–492 https://doi.org/10.1038/nature03090
2. Nomura, K., Takagi, A., Kamiya, T., Ohta, H., Hirano, M., Hosono, H. (2006). Amorphous oxide semiconductors for high-perfor mance flexible thin-film transistors. Jpn. J. Appl. Phys. 45, 4303 4308 https://doi.org/10.1143/jjap.45.4303
3. Park, J.S., Jeong, J.K., Mo, Y.G., Kim, H.D., Kim, S. (2007). Il: improvements in the device characteristics of amorphous indium gallium zinc oxide thin-film transistors by Ar plasma treatment. Appl. Phys. Lett. 90, 2012–2015 https://doi.org/10.1063/1.2753107
4. Olziersky, A., Barquinha, P., Vila, A., Magana, C., Fortunato, E., Morante, J.R., Martins, R. (2011). Role of Ga2O3–In2O3–ZnO chan nel composition on the electrical performance of thin-film tran sistors. Mater. Chem. Phys. 131, 512–518 https ://doi. org/10.1016/j.matchemphys.2011.10.013
5. Oh, H., Yoon, S.M., Ryu, M.K., Hwang, C.S., Yang, S., Park, S.H.K. (2010). Photon-accelerated negative bias instability involving subgap states creation in amorphous In-Ga-Zn-O thin film transis tor. Appl. Phys. Lett. https://doi.org/10.1063/1.3510471
6. Adaika, M., Meftah, A., Sengouga, N., Henini, M. (2015). Numerical simulation of bias and photo stress on indium-gallium-zinc-oxide thin film transistors. Vacuum 120, 59–67. https ://doi. org/10.1016/j.vacuum.2015.04.021
7. Kim, Y., Kim, S., Kim, W., Bae, M., Jeong, H.K., Kong, D., Choi, S., Kim, D.M., Kim, D.H. (2012). Amorphous InGaZnO thin film transistors—part II: modeling and simulation of negative bias illumination stress-induced instability. IEEE Trans. Electron Devices 59, 2699–2706. https ://doi.org/10.1109/ TED.2012.2208971
8. Ueoka, Y., Ishikawa, Y., Bermundo, J.P., Yamazaki, H., Urakawa, S., Fujii, M., Horita, M., Uraoka, Y. (2014). Density of states in amorphous In Ga-Zn-O thin-film transistor under negative bias illumination stress. ECS J. Solid State Sci. Technol. 3, Q3001–Q3004. https :// doi.org/10.1149/2.001409jss
9. Kamiya, T., Nomura, K., Hosono, H. (2010). Present status of amorphous In–Ga–Zn–O thin-film transistors. Sci. Technol. Adv. Mater. 11, 044305 https://doi.org/10.1088/1468-6996/11/4/044305
10. Fichtner, W., Rose, D.J.D.J., Bank, R.E.R.E. (1983). Semiconductor device simulation. IEEE Trans. Electron Devices 30, 1018–1030 https://doi.org/10.1109/T-ED.1983.21256
11. Park, J.C., Lee, H.-N., Chul, J. (2012). Dry etch damage and recovery of gallium indium zinc oxide thin-film transistors with etch-back struc tures. Displays 33, 133–135. https://doi.org/10.1016/j.displ a.2012.05.001
12. Kim, E., Kim, C.K., Lee, M.K., Bang, T., Choi, Y.K., Park, S.H.K., Choi, K.C. (2016). Influence of the charge trap density distribution in a gate insulator on the positive-bias stress instability of amorphous indium-gallium-zinc oxide thin-film transistors. Appl. Phys. Lett. 108, 1–6 https://doi.org/10.1063/1.4948765
13. Sisman, Z., Bolat, S., Okyay, A.K. (2017). Atomic layer deposition for vertically integrated ZnO thin film transistors: toward 3D high packing density thin film electronics. Phys. Status Solidi C 14, 1700128 https://doi.org/10.1002/pssc.201700128
14. Chun, Y.S., Chang, S., Lee, S.Y. (2011). Effects of gate insulators on the performance of a-IGZO TFT fabricated at room temperature. Micro electron. Eng. 88, 1590–1593. https ://doi.org/10.1016/j. mee.2011.01.076
15. Yuan, L., Zou, X., Fang, G., Wan, J., Zhou, H., Zhao, X. (2011). High-performance amorphous indium gallium zinc oxide thin-film transistors with HfO × N y/HfO 2/HfO × N y tristack gate dielectrics. IEEE Electron. Device Lett. 32, 42–44 https://doi.org/10.1109/ LED.2010.2089426
16. Kim, E., Kim, C.K., Lee, M.K., Bang, T., Choi, Y.K., Park, S.H.K., Choi, K.C. (2016). Influence of the charge trap density distribution in a gate insulator on the positive-bias stress instability of amorphous indium-gallium-zinc oxide thin-film transistors. Appl. Phys. Lett. 108, 1–6 https://doi.org/10.1063/1.4948765
17. Sisman, Z., Bolat, S., Okyay, A.K. (2017). Atomic layer deposition for vertically integrated ZnO thin film transistors: toward 3D high packing density thin film electronics. Phys. Status Solidi C 14, 1700128 https://doi.org/10.1002/pssc.201700128
18. Robertson, J. (2002). Band offsets of high dielectric constant gate oxides on silicon. J. Non Cryst. Solids 303, 94–100 https ://doi. org/10.1016/S0022-3093(02)00972-9
19. Gervais, F. (1998). Aluminum oxide (Al2O3). In: Palik, E.D. (ed.) Handbook of Optical Constants of Solids, pp. 761–775. Academic Press, Boston
20. Rignanese, G.-M., Gonze, X., Jun, G., Cho, K., Pasquarello, A. (2004). First-principles investigation of high-k dielectrics: comparison between the silicates and oxides of hafnium and zirconium. Phys. Rev. B. 69, 184301. https ://doi.org/10.1103/PhysR evB.69.184301
21. K. Myny, (2018). Nat. Electron 1, 30
22. M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K.Kuribara, T. Tokuhara, M. Drack, R.

Schwödiauer, I.Graz, S.B. Gogonea, S. Bauer, and T. Someya, (2013). Nature 499,458.
23. K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, (2013). Nature 432, 488–492.
24. R.L. Hoffman, B.J. Norris, and J.F. Wager (2003). Appl. Phys.Lett. 82, 733.
25. Y. Zhou (2020). (Ed), Semiconducting Metal Oxide Thin-Film Transistors, Institute of Physics Publishing (IOP), Bristol.
26. S.Y. Lee, (2020). Trans. Electr. Electron. Mater 21, 235.
27. J.F. Wager, (2020). Inform. Display 36, 9.
28. J. Souk, S. Morozumi, F.-C. Luo, and I. Bita,(2018) Flat PanelDisplay Manufacturing (Wiley, Hoboken).

AUTHORS

Akshay Verma received his BTech degree from A.K.T.U, Uttar Pradesh, India in 2022 and his M.Tech degree in VLSI Design from Dr B R Ambedkar National Institute of Technology Jalandhar Punjab, India in 2024.

E-mail: akshay2018verma@gmail.com

Nitesh Kashyap is currently Assistant Professor in the Department of Electronics & Communication Engineering, Dr B R Ambedkar National Institute of Technology, Jalandhar. He has completed his Ph.D. in Antenna Designing from PDPMIIITDM Jabalpur. His research interests are Antenna Engineering- EBG based antenna, Beamforming Antenna, Shared Aperture Antenna, Conformal Antenna, Graphene antenna, Metamaterial Based Antenna, Filtenna. RF and Microwave components and systems- Filters, couplers, power divider, phase shifter, circulator.

E-mail: kashyapn@nitj.ac.in