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ASIC Implementation of Vending Machine for Blood Pressure Medicine

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ABSTRACT

This paper presents the design and implementation of an Application-Specific Integrated Circuit (ASIC) for a vending machine tailored specifically for dispensing blood pressure medication. Hypertension, or high blood pressure, is a prevalent health concern globally, necessitating the need for efficient and accessible distribution of medication. The proposed ASIC-based vending machine offers a novel solution to address this need by providing a convenient and automated system for patients to obtain their prescribed blood pressure medication. The vending machine design leverages ASIC technology to achieve compactness, low power consumption, and high reliability. The system architecture comprises several key components, including a user interface for interaction, and a medication dispensing mechanism. This medication dispensing mechanism provides three different medicines (0.5mg, 5mg, and 50mg) for blood pressure relaxation. The proposed chip of the vending machine is implemented using Verilog HDL on the Xilinx ISE design suite. Three different FPGAs (Virtex 5, Spartan 3E, and Spartan 6) are used for the synthesis of the proposed circuit.

KEYWORDS

Vending Machine; ASIC; Verilog HDL; VLSI; Medicine; FPGA

1. INTRODUCTION

High blood pressure, or hypertension, is a prevalent cardiovascular condition affecting millions worldwide [1]-[4]. Effective management of hypertension often necessitates regular medication intake. However, accessing prescribed medication can sometimes pose challenges, particularly for individuals with busy schedules or limited mobility. In response to this issue, innovative solutions leveraging technology have emerged to streamline the dispensing process and improve medication adherence [5]-[7]. The traditional process of obtaining medication often involves visiting a pharmacy, which can be time-consuming and inconvenient, especially for individuals with mobility issues or those residing in remote areas. Furthermore, adherence to prescribed medication regimens poses a significant challenge, with studies indicating suboptimal adherence rates among patients with chronic conditions such as hypertension [8]-[11]. Factors contributing to medication non-adherence include forgetfulness, complex dosing schedules, and difficulty accessing pharmacies.

One such solution is the Application-Specific Integrated Circuit (ASIC)-based vending machine tailored for dispensing blood pressure medication. This vending machine represents a convergence of healthcare and engineering, offering a novel approach to medication distribution that prioritizes convenience, accessibility, and patient empowerment [12]-[16]. The ASIC-based vending machine presents a promising solution to address these challenges. By leveraging custom semiconductor technology, the vending machine offers a streamlined and user-friendly platform for patients to access their blood pressure medication conveniently. Equipped with advanced features such as user authentication, prescription verification, and dose customization, the vending machine ensures accuracy and

safety in medication dispensing while empowering patients to take control of their healthcare journey [17]-[23]. Moreover, the integration of secure payment processing modules enables cashless transactions, enhancing the efficiency and security of the dispensing process. Additionally, remote monitoring capabilities allow healthcare providers to track medication adherence remotely, providing valuable insights into patient behavior and enabling timely interventions when necessary.

The development and implementation of an ASIC-based vending machine for blood pressure medication signify a paradigm shift in healthcare delivery, where technology plays a central role in promoting patient-centric care and improving health outcomes. By combining engineering expertise with medical knowledge, this innovative approach holds the potential to revolutionize medication access and management, ultimately leading to better health outcomes and enhanced quality of life for individuals with hypertension.

By leveraging ASIC technology in the implementation of a vending machine for blood pressure medicine, manufacturers can achieve a highly optimized and reliable solution tailored to the specific requirements of the healthcare industry. Customized control, sensor interfaces, motor control, communication, security, power management, and form factor optimization are key aspects where ASICs can provide significant advantages over generic off-the-shelf components.

In the subsequent sections of this paper, we delve into the technical aspects of ASIC design, system architecture, functionalities, implementation challenges, and evaluation methodologies associated with the vending machine for blood pressure medicine. Section 2 includes comprehensive analysis, experimentation, and implementation of machines with the aim to elucidate the efficacy and feasibility of this

novel healthcare technology, paving the way for its adoption in clinical settings and beyond. FPGA-based synthesis and simulation results of the designed Vending machine are presented in Section 3. Section 4 concludes the work and suggests the future scope of the work.

2. Proposed Design of Vending Machine

The ASIC implementation of a vending machine for blood pressure medicine demands a structured methodology encompassing various stages, each critical for ensuring functionality, efficiency, and regulatory compliance [24]-[29]. Initially, comprehensive requirement analysis is conducted, delineating functional necessities such as medicine types, user interface specifications, and payment processing mechanisms, alongside non-functional aspects like power consumption limits and regulatory obligations. Following this, the system architecture is meticulously designed, outlining the interconnection of major components and interfaces with external systems, like payment networks and inventory management. Fig. 1 depicts the complete process of implementation of a Semi-Custom chip for a Vending machine.

With the architectural blueprint in place, the ASIC design planning commences, determining crucial factors such as technology nodes, performance metrics, and resource allocation. The subsequent phase entails the digital logic design, where hardware description languages like Verilog HDL are employed to develop the intricate logic required for vending machine functionalities. This design is then validated through simulation to ensure it meets the specified requirements and adheres to industry standards and regulatory frameworks.

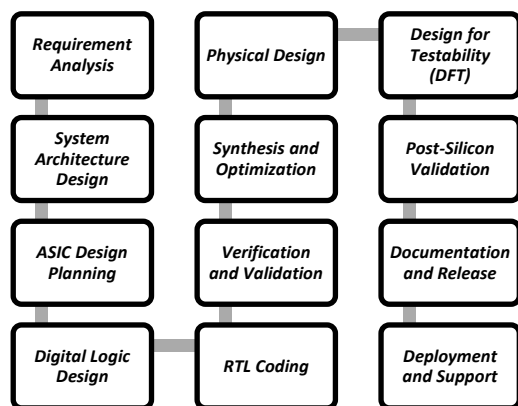


Fig. 1 Steps involved in ASIC implementation

Upon successful verification, the RTL (Register Transfer Level) code undergoes synthesis, transforming it into a gate-

level netlist optimized for timing, power, and area. Concurrently, physical design tasks, including floor planning, placement, and routing, are executed to generate the layout of the ASIC, addressing challenges such as clock distribution and signal integrity [30]- [36]. Design for Testability (DFT) techniques are integrated to facilitate manufacturing testing and fault diagnosis, ensuring the ASIC's robustness and ease of maintenance.

The methodology for ASIC implementation of a vending machine for blood pressure medicine involves several key steps in the design, verification, synthesis, and testing phases. Following the completion of physical design, prototype ASICs are fabricated for post-silicon validation, where functionality, performance, and reliability are verified through rigorous testing and compliance assessments [37]- [43]. Comprehensive documentation detailing the design process, verification results, and implementation specifics is prepared, culminating in the release of the ASIC design for manufacturing. Finally, support is extended for the deployment of the vending machine ASIC, encompassing ongoing maintenance, updates, and technical assistance to ensure its seamless integration and operation in real-world environments. Through adherence to this structured methodology, ASIC designers can navigate the complexities inherent in vending machine implementations, delivering robust, efficient, and compliant solutions tailored to the unique requirements of blood pressure medicine dispensing.

Fig. 2 shows the flow chart of the Vending machine specification for blood pressure medicine. This flow diagram depicts how the state diagram of blood pressure medicine Vending works. Based on higher blood pressure (Systolic) and lower blood pressure (Diastolic) values, the vending machine provides medicines and the status of the patient's condition is normal or not. When the range of higher blood pressure (Systolic) value is lower than 130 and lower blood pressure (Diastolic) value is greater than 70 and less than 130, no medicine is required. Similarly, When the range of higher blood pressure (Systolic) value is greater than or equal to 130 and lower blood pressure (Diastolic) value is greater than 70 and less than 130, 0.5mg medicine is required. When the range of higher blood pressure (Systolic) value is greater than or equal to 140 and lower blood pressure (Diastolic) value is greater than 70 and less than 130, 5mg medicine is required. When the range of higher blood pressure (Systolic) value is greater than or equal to 150 and lower blood pressure (Diastolic) value is greater than 70 and less than 130, 50mg medicine is required.

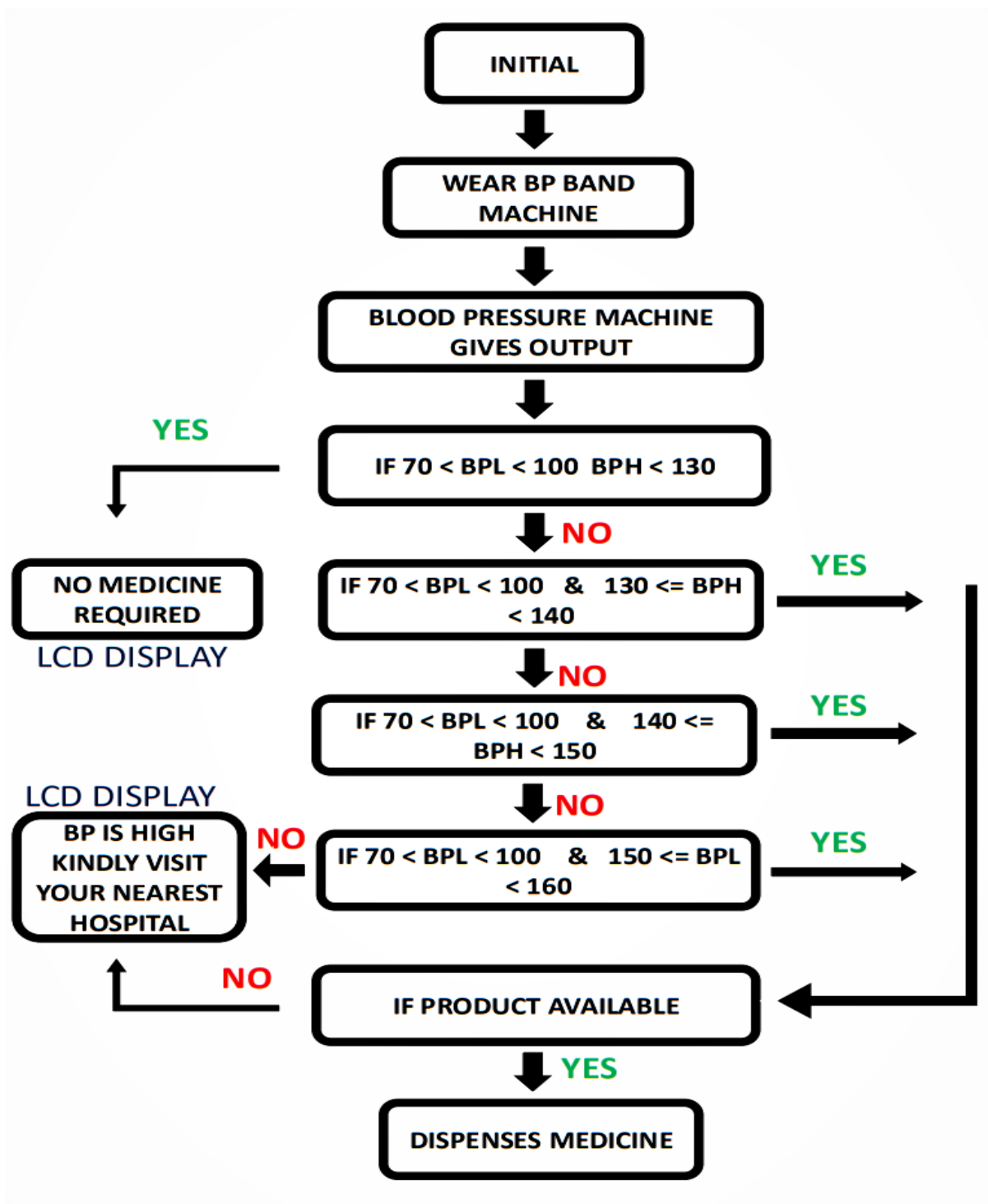


Fig. 2 Flow chart of ASIC implementation of vending machine for Blood pressure Medicine.

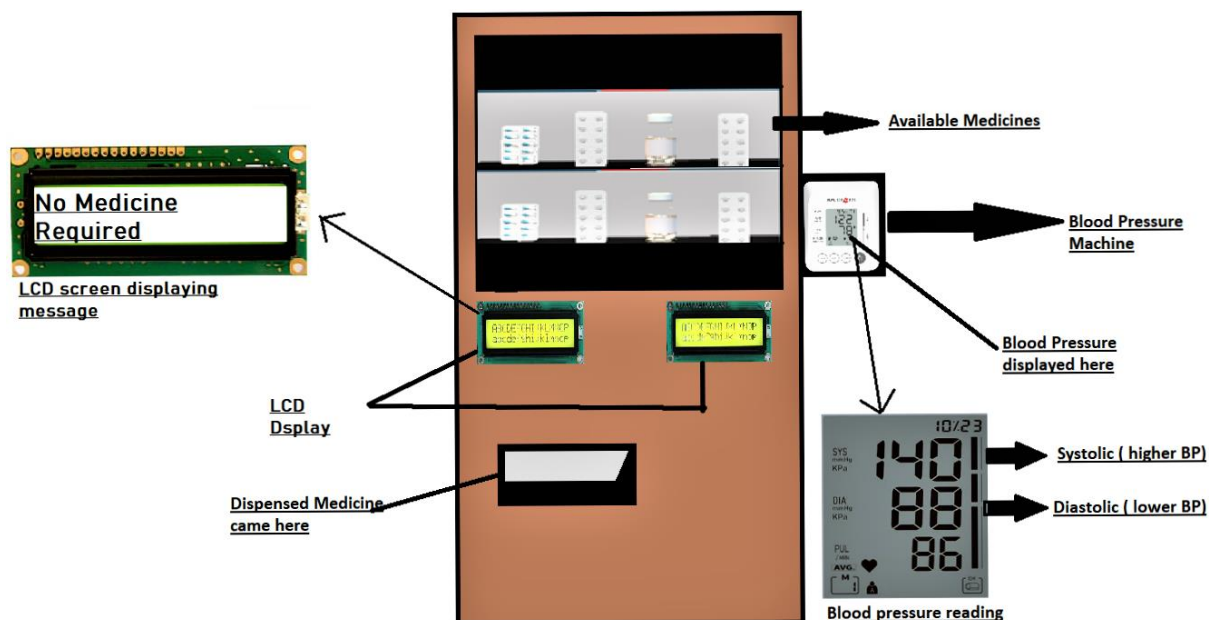


Fig. 3 Presupposition Diagram of the proposed vending machine.

Fig. 3 represents the presupposition diagram of the proposed blood pressure vending machine. Specification requirements for the blood pressure medicine vending machine are Medication Dispensing, User Interface, Authentication and Prescription Verification, Payment Processing, and Inventory Management. Accurate dispensing of blood pressure medication in prescribed dosages. Compatibility with various medication formulations (e.g., tablets, capsules). Ability to dispense multiple medications if needed. Ensuring tamper-proof packaging to maintain medication integrity like intuitive and user-friendly interface for patients of all ages and abilities, Touch screen display with clear instructions for medication selection and dosage customization, Option for audio instructions or accessibility features for visually impaired users, Language options to accommodate diverse user populations, Support for various payment methods, including cashless transactions (credit/debit cards, mobile payments), Secure payment processing protocols compliant with industry standards (e.g., PCI-DSS), Option for insurance billing integration to facilitate reimbursement for medication costs, Automated monitoring of medication stock levels to prevent stockouts. Alerts and notifications for low inventory levels or expired medications. Ability to track medication usage and refill history for inventory management purposes.

3. Result and Discussion

The RTL coding of the proposed blood pressure medicine vending machine, Verilog hardware description language (HDL) is used in this work. Synthesis of the proposed work has been done on commercially available FPGA (Virtex 5, Spartan 3E, and Spartan 6). Xilinx ISE design suit is used in this work for simulation and synthesis of proposed work. Fig. 4 presents the schematic diagram of the proposed vending

machine. Fig. 5 shows the detailed schematic diagram of the proposed Vending machine. Fig. 5 shows the detailed schematic diagram of the proposed Vending machine.

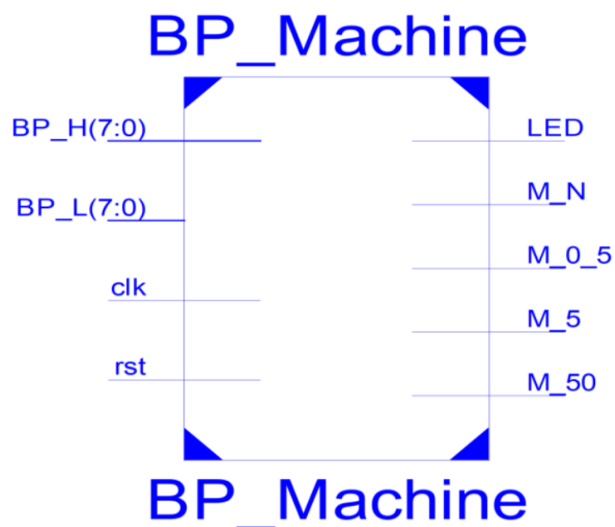


Fig. 4 Schematic Diagram of Vending Machine.

Creating a Register Transfer Level (RTL) schematic for the ASIC implementation of a vending machine for blood pressure medicine involves detailing the digital logic design at a low level. It includes the representation of state transitions and control logic using FSMs and, the representation of storage elements such as registers and flip-flops.

Signals line in schematics diagram represents the unique meaning: *BP_H*: Higher Blood pressure (Systolic), *BP_L*:

Lower Blood pressure (Diastolic), *CLK*: Clock Signal, *RST*: Reset, *LED*: Indicates LED Screen, *M_N*: No medicine

required, *M_0_5*: Medicine required of 0.5 mg, *M_5*: Medicine required of 5mg and *M_50*: Medicine required of 50mg.

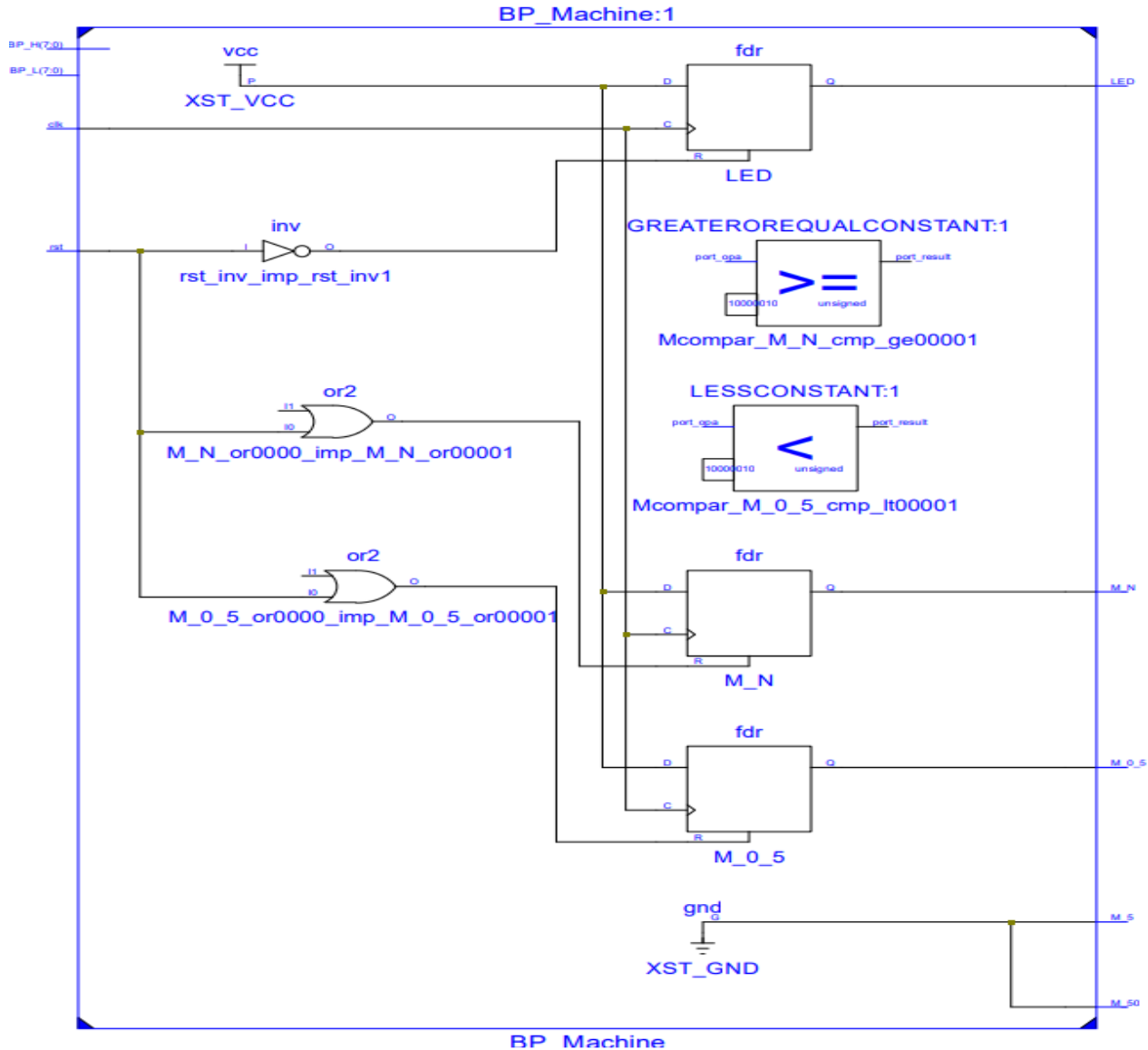


Fig. 5 Detailed Schematic Diagram of Vending Machine.

The RTL schematic serves as a blueprint for the digital logic design of the vending machine ASIC, guiding the implementation process and facilitating verification and synthesis. It provides a detailed visualization of the system architecture and operation, enabling designers to understand and refine the design efficiently.

The technology schematic for an ASIC implementation of a vending machine for blood pressure medicine is shown in Fig. 6. It involves specifying the semiconductor fabrication process and the physical layout of the integrated circuit. Here's an overview of what the technology schematic might include: Details of the process node and specific manufacturing techniques employed and a representation of the layout of transistors and interconnects on the silicon wafer. Allocation of logic gates and macroblocks on the silicon die Implementation of clock distribution networks to deliver clock

signals to various parts of the ASIC. The technology schematic provides a detailed representation of the physical implementation of the ASIC, guiding the fabrication process and ensuring that the design meets performance, power, and area requirements. It serves as a blueprint for semiconductor fabrication engineers and helps ensure the successful manufacturing of the ASIC.

Fig. 7(a) to Fig. 7(d) show the simulation waveform with different time instants of the proposed vending machine for high blood medicine. The signals line in simulation waveform represent the unique meaning *BP_H*: Higher Blood pressure (Systolic) reading, *BP_L*: Lower Blood pressure (Diastolic) reading, *CLK*: Clock Signal, *RST*: Reset, *LED*: Indicates to display the status on LED Screen, *M_N*: No medicine required, *M_0_5*: Medicine required of 0.5 mg, *M_5*: Medicine required of 5mg and *M_50*: Medicine required of 50mg.

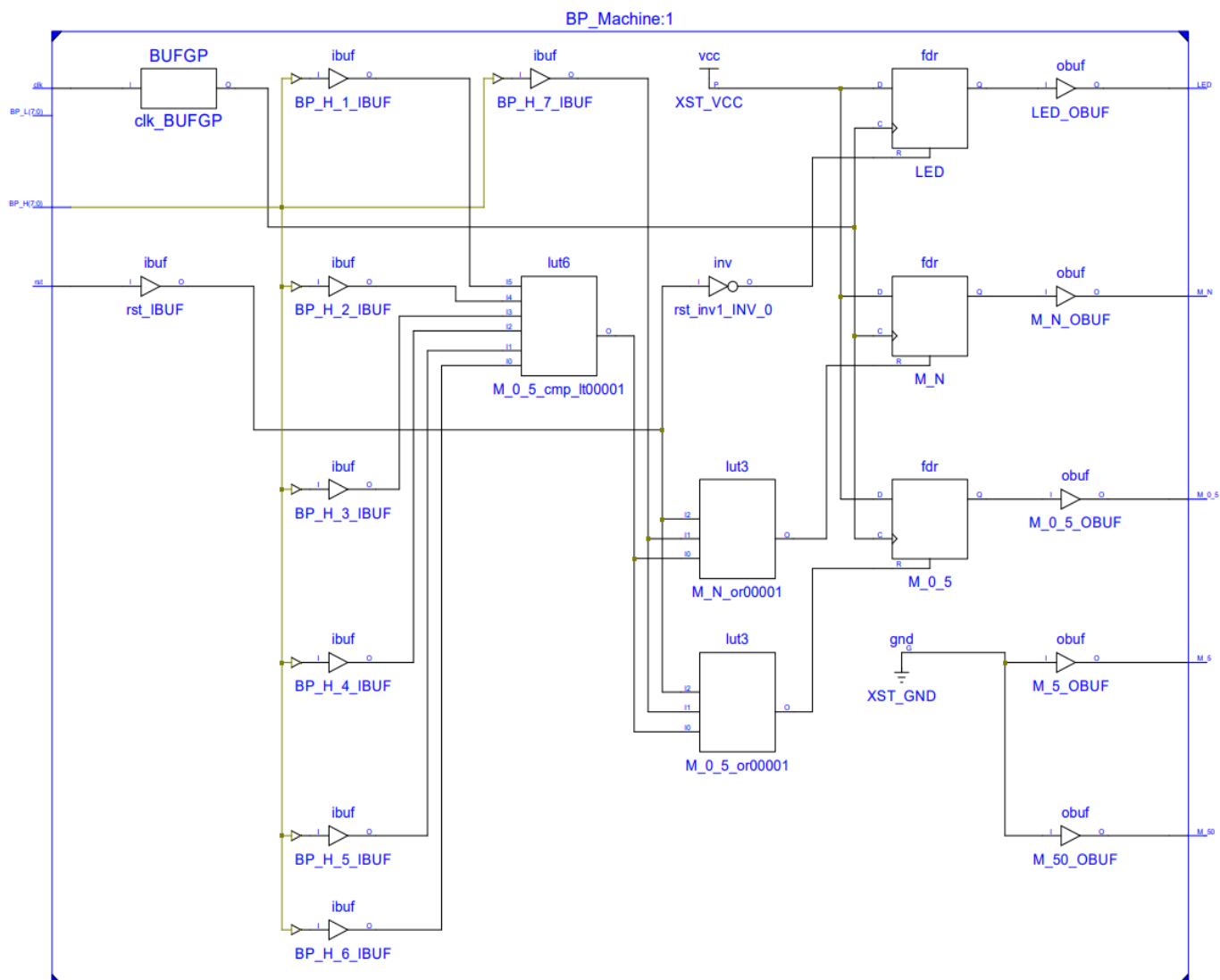
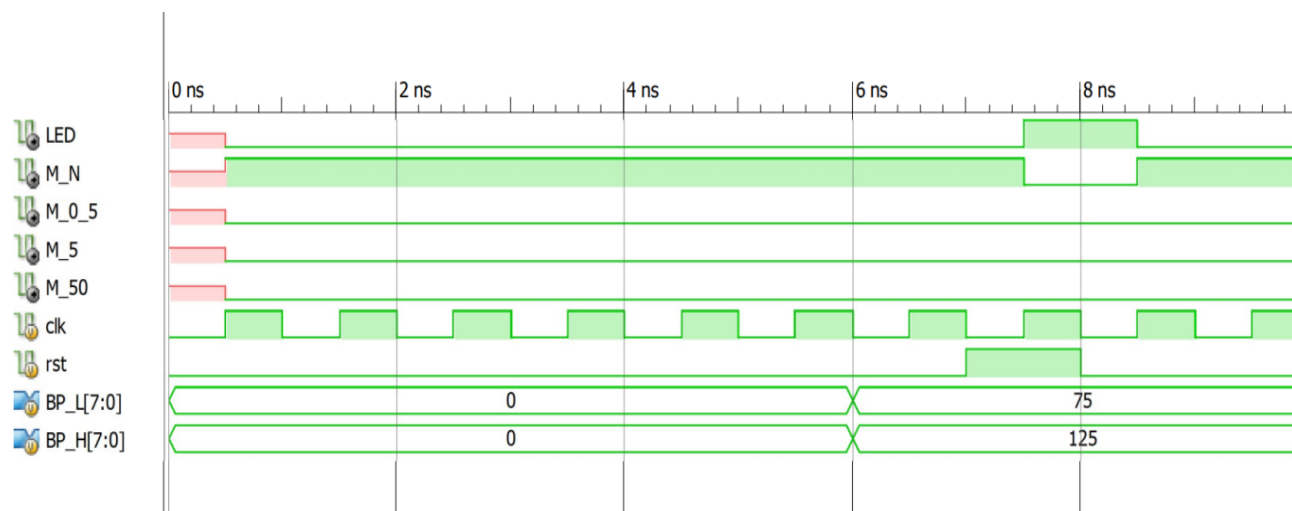
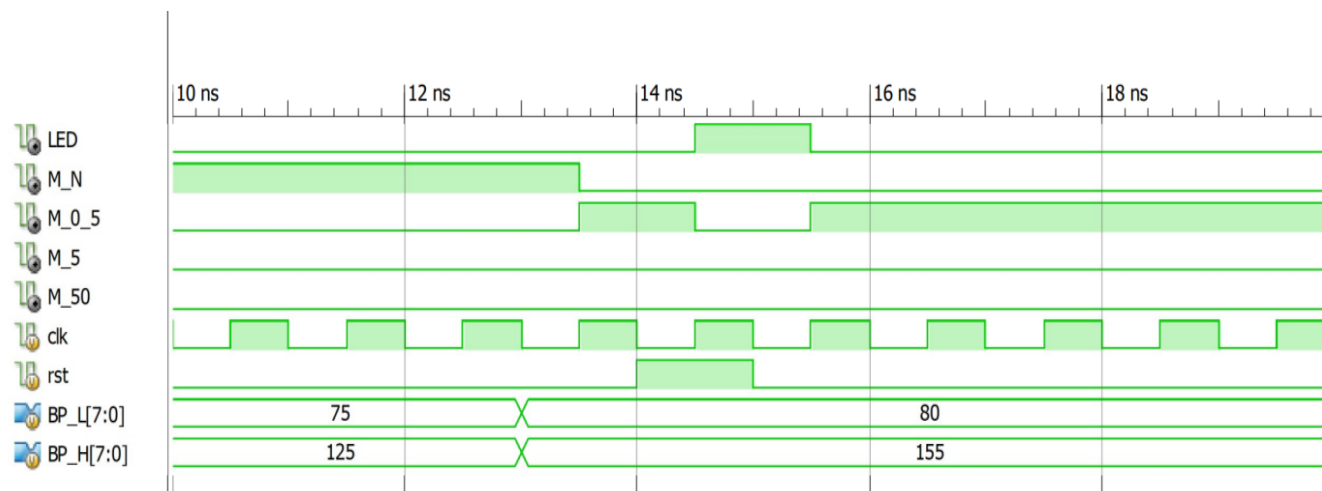


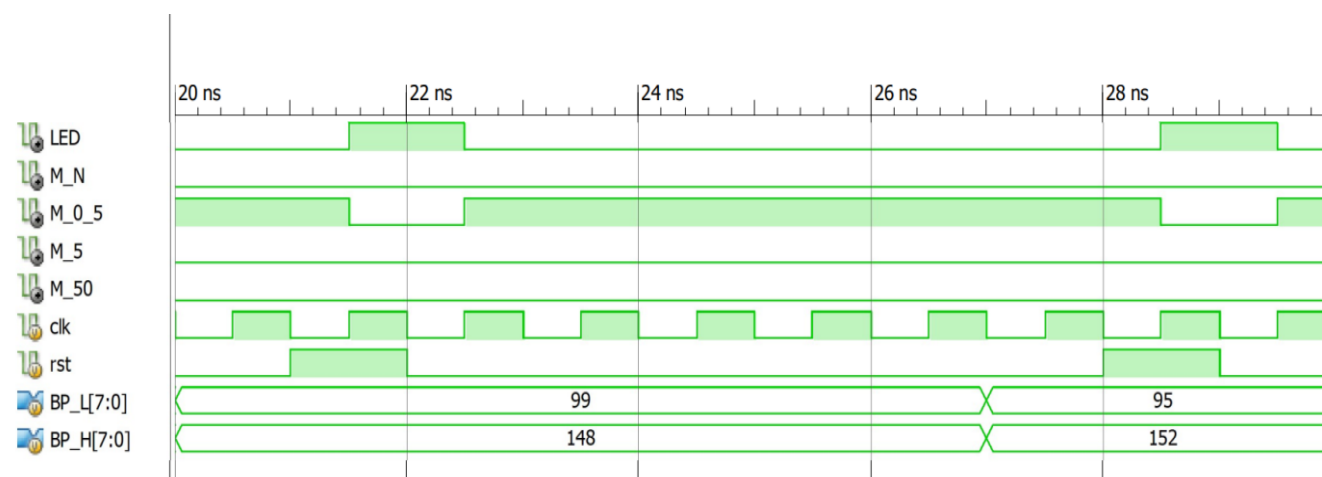
Fig. 6 Detailed Technology Schematic Diagram of Vending Machine.



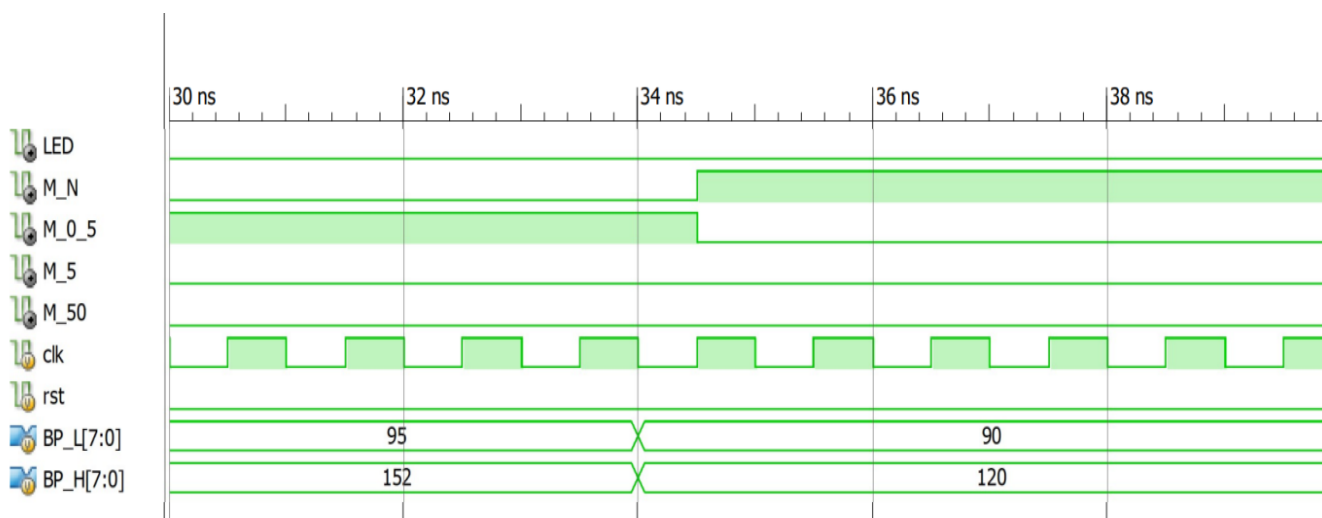
(a)



(b)



(c)



(d)

Fig. 7 Simulation waveform (a) to (d) of a Vending machine with different time scales.

Simulating the ASIC implementation of a vending machine for blood pressure medicine involves running tests to verify

the functionality and performance of the system. Here's a breakdown of what the simulation results might entail.

Table 1 presents the synthesis report of the proposed blood pressure medicine vending machine corresponding to three different FPGAs: Virtex-5, Spartan-3E, and Spartan-6. This table also compares the hardware performance in terms of utilized area (in terms of Slices, LUTs, and FFs) and timing performance (critical path delay) corresponding to three different FPGAs.

Therefore, the Designed ASIC chip of the blood pressure medicine vending machine integrates with an advanced sensor that enables personalized medication dispensing and real-time health monitoring capabilities. This design can collaborate with healthcare professionals and regulatory authorities is crucial to ensure compliance with industry standards and regulations governing medical devices.

Table 1: FPGA synthesis result of the proposed vending machine.

	FPGA Board		
	Virtex-5 (XC5VLX20 T-2FF323)	Spartan 3E (XC3S100 E- 5VQ100)	Spartan 6 (XC6SLX 4- 3TQG144)
Slice LUTs	9	-	11
Slices	-	7	-
4-input LUTs	-	12	-
Flip Flop/latch es	5	5	5
Delay	2.826ns	4.040ns	3.597ns

4. CONCLUSION

The ASIC implementation of a vending machine for dispensing blood pressure medicine represents a significant advancement in healthcare technology, offering patients greater accessibility to essential medications while streamlining the medication distribution process. Through a systematic methodology encompassing requirement analysis, design, verification, synthesis, and validation, ASIC designers can develop robust and efficient solutions tailored to the unique requirements of medical vending machines. This vending machine ASICs can ensure patient safety, data security, and operational reliability. It also represents a convergence of technology and healthcare, empowering patients with greater access to vital medications and fostering a more efficient and patient-centric healthcare delivery system. Therefore, the future scope for ASIC implementation of vending machines for blood pressure medicine is promising, with several avenues for integration with the healthcare ecosystem, and expanded medication options. Vending machines can be integrated into the broader healthcare

ecosystem, facilitating seamless communication with electronic health records, pharmacy systems, and telemedicine platforms. This integration enables healthcare providers to access patient medication history, prescribe medications remotely, and monitor treatment outcomes. The proposed vending machines have the potential for global adoption, particularly in underserved areas with limited access to healthcare facilities. Future efforts should focus on making these vending machines affordable, scalable, and adaptable to different healthcare contexts and regulatory environments.

REFERENCES

- Arguedas, J. A., Perez, M. I., & Wright, J. M. (2009). Treatment blood pressure targets for hypertension. *Cochrane Database of Systematic Reviews*, 3. <https://doi.org/10.1002/14651858.CD004349.pub2>
- Obisesan, T. O., Obisesan, O. A., Martins, S., Alamgir, L., Bond, V., Maxwell, C., & Gillum, R. F. (2008). High blood pressure, hypertension, and high pulse pressure are associated with poorer cognitive function in persons aged 60 and older: The Third National Health and Nutrition Examination Survey. *Journal of the American Geriatrics Society*, 56(3), 501–509. <https://doi.org/10.1111/j.1532-5415.2007.01592.x>
- Kadiri, S., Walker, O., Salako, B. L., & Akinkugbe, O. (1999). Blood pressure, hypertension and correlates in urbanised workers in Ibadan, Nigeria: A revisit. *Journal of Human Hypertension*, 13(1), 23–27. <https://doi.org/10.1038/sj.jhh.1000722>
- Hermansen, K. (2000). Diet, blood pressure and hypertension. *British Journal of Nutrition*, 83(SUPPL. 1), S113–S119. <https://doi.org/10.1017/s0007114500001045>
- Elias, P. K., Ralph, D. D., Elias, M. F., & Wolf, P. A. (1995). Blood pressure, hypertension, and age as risk factors for poor cognitive performance. *Experimental Aging Research*, 21(4), 393–417. <https://doi.org/10.1080/03610739508253992>
- Strelec, M. A. A. M., Pierin, A. M. G., & Mion, D. (2003). The influence of patient's consciousness regarding high blood pressure and patient's attitude in face of disease controlling medicine intake. *Arquivos Brasileiros de Cardiologia*, 81(4), 349–354. <https://doi.org/10.1590/s0066-782x2003001200002>
- Banegas, J. R., Segura, J., Sobrino, J., Rodríguez-Artalejo, F., de La Sierra, A., de La Cruz, J. J., Gorostidi, M., Sarria, A., & Ruilope, L. M. (2007). Effectiveness of blood pressure control outside the medical setting. *Hypertension*, 49(1), 62–68. <https://doi.org/10.1161/01.HYP.0000250557.63490.55>
- Hinton, T. C., Adams, Z. H., Baker, R. P., Hope, K. A., Paton, J. F. R., Hart, E. C., & Nightingale, A. K. (2020). Investigation and Treatment of High Blood Pressure in Young People: Too Much Medicine or Appropriate Risk Reduction? *Hypertension* (Dallas, Tex. : 1979), 75(1), 16–22. <https://doi.org/10.1161/HYPERTENSIONAHA.119.13820>
- Schwartz, J. E., Pickering, T. G., & Landsbergis, P. A. (1996). Work-related stress and blood pressure: current theoretical models and considerations from a behavioral medicine perspective. In *Journal of occupational health psychology* (Vol. 1, Issue 3, pp. 287–310). Educational Publishing Foundation. <https://doi.org/10.1037/1076-8998.1.3.287>
- Kannel, W. B. (1996). Blood Pressure as a Cardiovascular Risk Factor. *Jama*, 275(20), 1571. <https://doi.org/10.1001/jama.1996.03530440051036>
- Ware, M. A. (2008). Complementary and Alternative Medicine Approaches to Chronic Pain. *Chronic Pain: A Health Policy Perspective*, 54(11), 153–165. <https://doi.org/10.1002/9783527622665.ch13>
- Sibanda, V., Munetsi, L., Mpofu, K., Murena, E., & Trimble, J. (2020). Design of a high-tech vending machine. *Procedia CIRP*, 91, 678–683. <https://doi.org/10.1016/j.procir.2020.04.133>
- Eeswarasai, Y. (2022). Design of Low Power Fsm Based Vending Machine Using Page No : 602 Vol 13 , Issue 05 , May / 2022 ISSN NO : 0377-9254 Page No : 603. 13(05), 602–606.
- GUPTA, M. D., CHAUHAN, R. K., & UPADHYAY, V. K. (2023). Analyses of Reconfigurable Chaotic Systems and their Cryptographic S-box Design Applications. *Chaos Theory and*

- Applications, 5(3), 219–232. <https://doi.org/10.51537/chaos.1285094>
15. Gupta, M. D., & Chauhan, R. K. (2022). Hardware Efficient Pseudo-Random Number Generator Using Chen Chaotic System on FPGA. *Journal of Circuits, Systems and Computers*, 31(3), 1–14. <https://doi.org/10.1142/S0218126622500438>
 16. Suthar, M. (2021). A Novel Implementation of FPGA Based Smart Vending Machine. 2021 IEEE International Conference on Technology, Research, and Innovation for Betterment of Society, TRIBES 2021, 1–6. <https://doi.org/10.1109/TRIBES52498.2021.9751636>
 17. Solano, A., Duro, N., Dormido, R., & González, P. (2017). Smart vending machines in the era of internet of things. *Future Generation Computer Systems*, 76, 215–220. <https://doi.org/10.1016/j.future.2016.10.029>
 18. Sati, R., Mishra, V., & Verma, G. (2022). Simulation of Vending Machine Design using Verilog HDL. 2022 2nd Asian Conference on Innovation in Technology, ASIANCON 2022, 1–5. <https://doi.org/10.1109/ASIANCON55314.2022.9909003>
 19. Verma, G., Papreja, A., Shekhar, S., Maheshwari, S., & Virdi, S. K. (2016). Low power implementation of FSM based vending machine on FPGA. *Proceedings of the 10th INDIACOM; 2016 3rd International Conference on Computing for Sustainable Global Development, INDIACOM 2016*, 2054–2058.
 20. Gupta, M. D., & Chauhan, R. K. (2023). Recent Development of Hardware-Based Random Number Generators on FPGA for Cryptography. In B. Mishra & M. Tiwari (Eds.), *Lecture Notes in Electrical Engineering* (Vol. 877, pp. 489–500). Springer Nature Singapore. https://doi.org/10.1007/978-981-19-0312-0_48
 21. Singh, S. K., Gupta, M. D., & Chauhan, R. K. (2021). Design and FPGA Synthesis of an Efficient Synchronous Counter with Clock-Gating Techniques. *Lecture Notes in Electrical Engineering*, 692, 277–288. https://doi.org/10.1007/978-981-15-7486-3_27
 22. Yang, C., & Xu, Y. (2022). Design and Implementation of Fruit and Vegetable Vending Machine Based on Deep Vision. In Q. Liu, X. Liu, B. Chen, Y. Zhang, & J. Peng (Eds.), *Lecture Notes in Electrical Engineering: Vol. 808 LNEE* (pp. 203–210). Springer Nature Singapore. https://doi.org/10.1007/978-981-16-6554-7_24
 23. Chidananda Datta, P., Vinay Kumar, C., Singh, R., & Mummaneni, K. (2023). Optimized RTL Design of a Vending Machine Through FSM Using Verilog HDL. In T. R. Lenka, D. Misra, & L. Fu (Eds.), *Lecture Notes in Electrical Engineering* (Vol. 904, pp. 305–316). Springer Nature Singapore. https://doi.org/10.1007/978-981-19-2308-1_32
 24. Gupta, M. D., Singh, S. K., & Chauhan, R. K. (2021). Design of High-Speed Binary Counter Architecture for Low-Power Applications. In *Lecture Notes in Electrical Engineering* (Vol. 692). Springer Singapore. https://doi.org/10.1007/978-981-15-7486-3_13
 25. Gupta, M. D., & Chauhan, R. K. (2021). Secure image encryption scheme using 4D-Hyperchaotic systems based reconfigurable pseudo-random number generator and S-Box. *Integration*, 81, 137–159. <https://doi.org/10.1016/j.vlsi.2021.07.002>
 26. Kumar, K. (2021). Design of vending machine through implementation of visual automata simulator and finite state machine. *International Journal of Research in Circuits, Devices and Systems*, 2(2), 60–64.
 27. Monga, A. (2012). Finite State Machine based Vending Machine Controller with Auto-Billing Features. *International Journal of VLSI Design & Communication Systems*, 3(2), 19–28. <https://doi.org/10.5121/vlsic.2012.3202>
 28. Ratnasri, N., & Sharmilan, T. (2021). Vending Machine Technologies: A Review Article. *International Journal of Sciences: Basic and Applied Research (IJSBAR)*, 58(2), 160–166. <https://www.gssr.org/index.php/JournalOfBasicAndApplied/article/view/12579>
 29. Brolin, A., Mithun, R., Gokulnath, V., & Harivishanth, M. (2018). Design of automated medicine vending machine using mechatronics techniques. *IOP Conference Series: Materials Science and Engineering*, 402(1), 12044. <https://doi.org/10.1088/1757-899X/402/1/012044>
 30. Gupta, M. D., & Chauhan, R. K. (2020). Design of Modified Dual-CLCG Algorithm for Pseudo-Random Bit Generator. *International Conference on Electrical and Electronics Engineering, ICE3 2020*, 391–395. <https://doi.org/10.1109/ICE348803.2020.9122818>
 31. Gupta, M. D., & Chauhan, R. K. (2020). Performance Investigation of Binary Counter with Different Clock Gating Networks. 12(2), 59–67.
 32. Kho, E., & Kumar, M. (2020). Design and Implementation of FPGA based Vending Machine for Integrated Circuit (IC). *Proceedings of the 2020 IEEE International Conference on Communication and Signal Processing, ICCSP 2020*, 4(7 SE-Articles), 246–251. <https://doi.org/10.1109/ICCSP48568.2020.9182375>
 33. Ramachandran, S. (Ed.). (2007). Projects Suggested for FPGA/ASIC Implementations. In *Digital VLSI Systems Design* (pp. 659–696). Springer Netherlands. https://doi.org/10.1007/978-1-4020-5829-5_15
 34. Ramzan, A., Rehman, S., & Perwaiz, A. (2017). RFID technology: Beyond cash-based methods in vending machine. 2017 2nd International Conference on Control and Robotics Engineering, ICCRE 2017, 189–193. <https://doi.org/10.1109/ICCRE.2017.7935068>
 35. Gupta, M. D., & Chauhan, R. K. (2021). Efficient Hardware Implementation of Pseudo-Random Bit Generator Using Dual-CLCG Method. *Journal of Circuits, Systems and Computers*, 30(10), 1–6. <https://doi.org/10.1142/S0218126621501826>
 36. Gupta, M. D., & Chauhan, R. K. (2021). Improved VLSI Architecture of Dual-CLCG for Pseudo-Random Bit Generator. *Lecture Notes in Electrical Engineering*, 676, 175–182. https://doi.org/10.1007/978-981-15-6229-7_14
 37. Qian, J., Liu, C., Ai, Y., Zhao, G., & Qian, X. (2025). Enhancing Automated Vending Machine Product Recognition Through Depth-Guided Regression Refinement. *IEEE Transactions on Industrial Informatics*, 1–11. <https://doi.org/10.1109/TII.2025.3545046>
 38. Murena, E., Sibanda, V., Sibanda, S., & Mpofu, K. (2020). Design of a Control System for a Vending Machine. *Procedia CIRP*, 91, 758–763. <https://doi.org/10.1016/j.procir.2020.04.136>
 39. Yokouchi, T. (2010). Today and tomorrow of vending machine and its services in Japan. 2010 7th International Conference on Service Systems and Service Management, *Proceedings of ICSSSM' 10*, 221–225. <https://doi.org/10.1109/ICSSSM.2010.5530240>
 40. Gupta, M. D., & Chauhan, R. K. (2021). Coupled variable-input LCG and clock divider-based large period pseudo-random bit generator on FPGA. *IET Computers and Digital Techniques*, 15(5), 349–361. <https://doi.org/10.1049/cdt.2.12027>
 41. Gupta, M. D., & Chauhan, R. K. (2021). Design of an efficient parallel comparator architecture for low power delay product. *Advances in Electrical and Electronic Engineering*, 19(2), 155–167. <https://doi.org/10.15598/aeee.v19i2.4101>
 42. Singh, S. K., Gupta, M. D., Mani, S., & Chauhan, R. K. (2020). Design of LFSR Circuit based on High Performance XOR gate. *International Conference on Electrical and Electronics Engineering, ICE3 2020*, 656–660. <https://doi.org/10.1109/ICE348803.2020.9122875>
 43. Gupta, M. D., Chauhan, R. K., & Gulia, S. (2023). Hardware Efficient Hybrid Pseudo-Random Bit Generator Using Coupled-CLCG and Multistage LFSR with Clock Gating Network. *Journal of Circuits, Systems and Computers*, 32(3), 1–24. <https://doi.org/10.1142/S0218126623500391>

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