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Design and Comparative Analysis of a Low-Power Subthreshold Folded Cascode Variable Gain Amplifier in 90 nm and 45 nm CMOS Technology

Tanmay Deuskar, Varun Shastry, and Pankaj Arora

Department of Electrical and Electronics Engineering, Birla Institute of Technology and Science, Pilani, Rajasthan, India.

ABSTRACT
Variable gain amplifiers have been of great research interest in recent years. With increasing applications in biomedical systems, it becomes essential to design low-power models of the same. This paper proposes an ultra-low power variable gain amplifier using a Gilbert Cell and provides a comparative analysis across 90 nm and 45 nm CMOS technologies. The proposed design operates at a supply voltage of 0.5 V and achieves an adjustable gain range with a maximum gain of 31 dB. This amplifier operates in the subthreshold region, enabling a power dissipation as low as 10 nW while maintaining a significantly large 3 dB bandwidth.

KEYWORDS
Variable gain amplifier;
Subthreshold;
Folded Cascode;
Gilbert Cell;
Low Power

1. INTRODUCTION

The rapid advancement of medical technology has heightened the demand for ultra-low-power analog circuits, particularly in biomedical applications. One such application is neural signal recording, which requires low-power amplifiers to process weak signals with high-quality amplification [1, 2]. These amplifiers are essential for the acquisition of the Central Nervous System (CNS) signals, as CNS signals are inherently weak and demand high-gain amplification [3]. The role of low-power amplifiers in neural sensing is shown in Figure 1. Other devices, such as cochlear processors and pacemakers, have stringent power budgets in the range of a few microwatts [4, 5]. Amplifiers in medical systems have low noise requirements as well as operational frequencies in the range of a few kilohertz (kHz). Electrocardiogram (ECG) signals typically range from 1 µV to 10 mV, with an operational bandwidth of 0.1 Hz to 1 kHz [6]. Signals that enable the monitoring of the neuro-electrical activity of the brain range in frequency up to 80 Hz [7].

Numerous existing works focus on achieving low-noise amplification at minimal power consumption, with differing approaches based on topology, technology node, and application domain. For instance, a Front End Amplifier (FEA) for neural signal applications is presented in [8]. This design is implemented using 180 nm technology and utilizes a cascoded differential amplifier to attain a high gain while maintaining a low power consumption of 7.6 µW. A technique of current compensation feedback is used to increase input impedance. Another design uses 65 nm CMOS technology to make a Variable Gain Amplifier (VGA), which finds use in stabilizing Low Noise Amplifier (LNA) outputs used in neural sensing [9].

The gain variation is achieved by using a constant G_m bias circuit. This design offers a gain range of 2 dB to 25 dB while consuming 0.75 mW of power. Additionally, an instrumentation amplifier intended for portable ECG applications is described in [10]. It utilizes 180 nm CMOS technology and offers a gain of 46 dB with a power consumption of 3.99 µW. The above works demonstrate the trade-offs between power, gain, and technology scaling across application domains.

As technology progresses, further reduction in power consumption and supply voltage becomes essential. This paper proposes an ultra-low-power (<1 µW) VGA to address the increasing demand for such topologies. The amplifier achieves this by exploiting the subthreshold region of operation. Contrary to classical theory, a small drain current still exists even when the gate-to-source voltage is below the threshold voltage. While designing low-power circuits, the drain current in the subthreshold region is of great importance. The drain current has an exponential dependence on the gate-to-source voltage, allowing for higher gain values than other low-power amplifiers that are biased in saturation. A folded cascode design, compared to a simple cascode, allows for higher input/output voltage swings while maintaining a significant bandwidth. The design also achieves a higher gain and is useful for cascading with more stages. This is achieved because the design introduces only a single dominant pole at a sufficiently high frequency.

Voltage control is implemented using a Gilbert cell. Using a Gilbert cell with MOSFETs biased in the subthreshold region allows for relative simplicity of operation while maintaining

the gain and bandwidth of the amplifier. The use of analog control voltages allows a gain variation of up to 30 dB. Apart from these figures of merit, the power supply rejection ratio (PSRR) and the common mode rejection ratio (CMRR) have also been simulated. In addition, we compare the effects of variation in technology on the simulated parameters. 90-nm and 45-nm process technologies have been considered in this work.

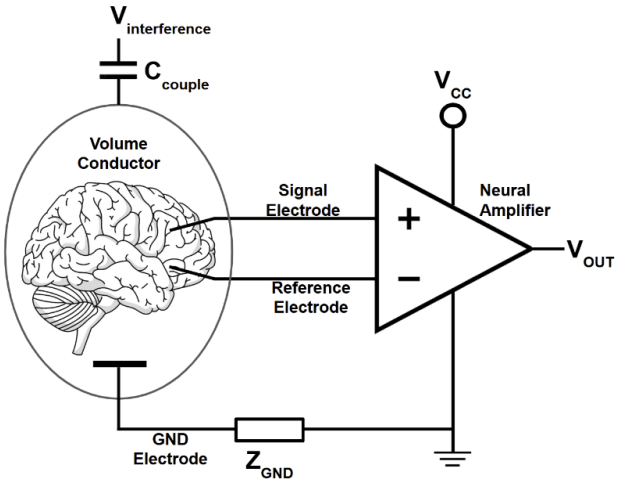

Fig. 1 Typical setup for neural recording [3]

2. Proposed Design

2.1 Subthreshold Region:

The subthreshold region of a MOSFET is the operational region where the gate-to-source voltage (V_{GS}) is lower than the threshold voltage (V_{th}). In this region, the drain current is significantly low, allowing circuits to operate with ultra-low power consumption. The drain current in the subthreshold region and the small signal characteristics are governed by the following equations [11, 12]:

$$I_{sub} = I_0 e^{\frac{V_{GS}-V_{th}}{\eta V_T}}\left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \quad (1)$$

for $V_{DS} > 3V_T$, this simplifies to:

$$I_{sub} \approx \frac{W}{L} I_0 exp\left(\frac{V_{GS}-V_{th}}{\eta V_T}\right) \quad (2)$$

Here, W/L is the aspect ratio, V_{GS} is the gate-to-source voltage, and V_{DS} is the drain-to-source voltage. The parameter I_0 is given by:

$$I_0 = \mu_0 C_{ox}\left(\frac{W}{L}\right) V_T^2 e^{1.8} \quad (3)$$

where μ_0 is the carrier mobility, C_{ox} is the gate oxide capacitance, and V_T is the thermal voltage (approximately 26 mV at room temperature). The parameter η (also called the subthreshold slope factor) is process-dependent.

The threshold voltage (V_{th}) is given by:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{V_{bs} + 2\phi_B} - \sqrt{2\phi_B}\right) \quad (4)$$

where V_{th0} is a process-dependent constant, Υ is the body effect coefficient, and Φ_B is the bulk potential.

The transconductance (g_m) in the subthreshold region is expressed as:

$$g_m = \frac{I_{sub}}{\eta V_T} \quad (5)$$

For small signal conditions:

$$v_{gs} \ll \eta V_T \quad (6)$$

The output resistance (r_o) of a MOSFET in the subthreshold region is given by:

$$r_o = \frac{1}{\eta g_m} \quad (7)$$

where η is the drain-induced barrier lowering coefficient.

The above equations indicate that operating a MOSFET in the subthreshold region enables low-power and high-gain amplification, making it particularly useful for biomedical and ultra-low-power analog applications.

2.2 Gilbert Cell:

The Gilbert cell is a topology that allows for the multiplication of two signals. This feature finds great use in RF circuits, where Gilbert cells are most commonly used. Gilbert cells can also be used in VGAs, where the output signal is the product of the input signal and a control voltage [13]. This control voltage can be used to vary the gain. Figure 2 shows the basic structure of a Gilbert cell.

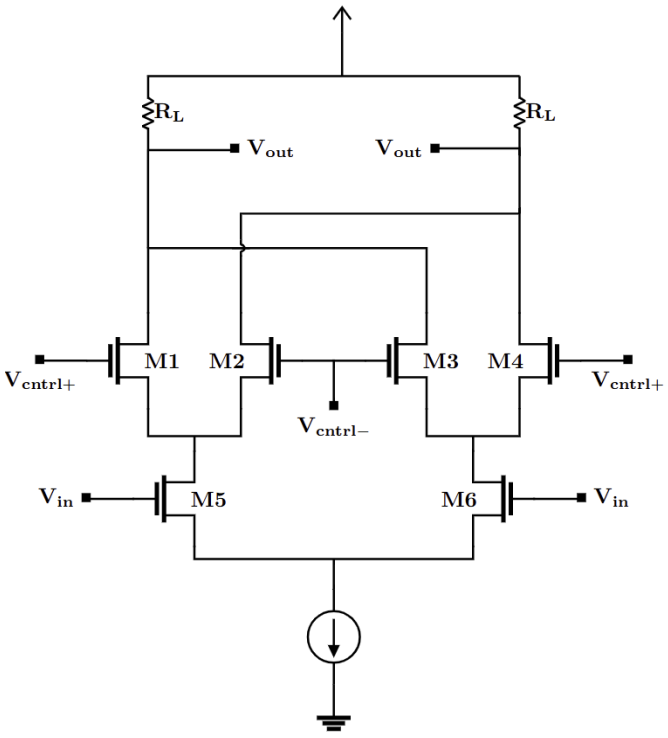

Fig. 2 Basic structure of a Gilbert Cell.

The Gilbert cell consists of three basic parts: the load stage, the switching stage (M1–M4), and the transconductance stage (M5, M6) [14, 15]. The differential gain of the circuit in the subthreshold region is given by the expression:

$$v_{out} = \frac{1}{\eta V_T}(g_{m5/6} v_{in}) v_{cntrl} R_L \quad (8)$$

Here, v_{cntrl} is the differential voltage applied to the V_{cntrl+} and V_{cntrl-} terminals.

Thus, the Gilbert cell provides a high degree of linearity in gain control, making it an essential building block in the design of VGAs.

2.3 Amplifier Topology:

The design of the amplifier circuit is presented in this section. This circuit utilizes a folded cascode topology, which incorporates a Gilbert cell for variable gain control. Folded cascode amplifiers provide high gain while allowing a greater output swing. This topology is also highly suitable for feedback and is optimal for cascading. Furthermore, the Gilbert cell allows for a wide range of gain control. The schematic is shown in Figure 3. The input signal is applied differentially to MOSFETs M9 and M10. The input range of v_{in} is determined by equation (6). MOSFETs M12-M15 form the Gilbert cell, to which the control voltages V_{cntrl+} and V_{cntrl-} are applied to vary the gain. MOSFETs M5-M8 form a current mirror, enabling a single-ended output. The load capacitance C_L is fixed at 10 fF so that it can be directly supplanted by the input capacitance of any cascaded stage.

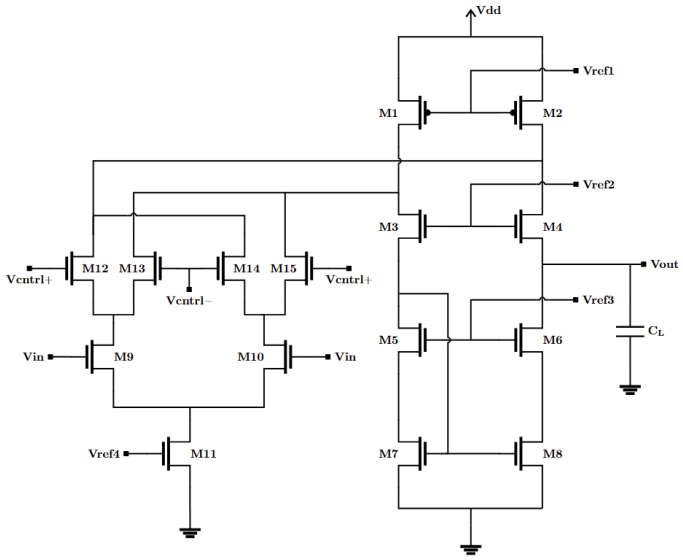

Fig. 3 Schematic of folded cascode variable gain amplifier.

The voltage gain of the amplifier is given by the expression:

$$A_v = -g_{m9}(g_{m6} r_{o6} r_{o8} \,||\, g_{m4} r_{o4}(r_{o2} \,||\, \frac{g_{m12} r_{o12} r_{o9}}{2})) \quad (9)$$

where g_m and r_o are given by Equations (5) and (7), respectively. The DC current is given by Equation (2).

In both the 90 nm and 45 nm technologies, V_{DD} is taken as 0.5 V, which is suitable for low-power devices. The drain current for each MOSFET was approximated based on the maximum allowed power dissipation and V_{DD}. Suitable aspect ratios and the reference voltages V_{ref1} through V_{ref4} were calculated with the aid of Equation (2). V_{ref4} is the bias for the tail current source, implemented by a basic current mirror. The DC offset for the input voltage and V_{cntrl} were also calculated similarly. The aspect ratios are presented in Table I, and the reference voltages are given in Table II.

Table I Aspect Ratios of MOSFETs

MOSFET	W/L for 45 nm	W/L for 90nm
M_1, M_2	3149n / 45n	2255n / 90n
M_3, M_4	1413n / 45n	1007n / 90n
M_5, M_6	1193n / 45n	677n / 90n
M_7, M_8	1613n / 45n	519n / 90n
M_9, M_{10}	822n / 45n	1133n / 90n
M_{11}	744n / 45n	1608n / 90n
M_{12}, M_{13}, M_{14}, M_{15}	2543n / 45n	2101n / 90n

Table II Reference Voltages and Bias Values

Parameter	45nm	90nm
V_{DD}	0.5V	0.5V
V_{ref1}	0.23V	0.26V
V_{ref2}	0.14V	0.19V
V_{ref3}	0.36V	0.31V
V_{ref4}	0.31V	0.22V
DC input voltage	0.42V	0.38V
Control Voltage (zero offset)	0.48V	0.46V

The total current in the 45 nm version is 20 nA; in the 90 nm iteration, it is 2 µA. This gives a power dissipation of 10 nW and 1 µW, respectively.

3. Simulation Results

This section presents the simulation results of the circuit in both 90 nm and 45 nm node technologies. The circuit presented in Figure 3 was simulated using SPICE software. Figure 4 shows the open-loop frequency response of the amplifier (for both technology nodes). The differential control voltage is set high

enough to ensure the maximum differential gain. It can be seen from Figure 4(a) that for the 45 nm node, the low frequency gain is 31.3 dB with a 3dB bandwidth of 247 kHz. The Unity Gain Bandwidth (UGB) is 2.9 MHz. Figure 4(b) shows that for the 90 nm node, the low-frequency gain is 25.24 dB. The 3 dB bandwidth is 55.7 MHz with a UGB of 353 MHz. The UGB of the folded cascode amplifier is given by equation (10).

$$UGB = \frac{g_{m9}}{C_L} \tag{10}$$

The transconductance g_m scales directly with subthreshold drain current as per Equation (5). The 90 nm version has MOSFETs M9/M10 biased at 0.7 µA, while the 45 nm version is biased at 6 nA. Thus, the higher g_m of the 90 nm iteration yields a higher bandwidth.

Figure 5 shows the low-frequency gain variation with differential control voltage. The plot for the 45 nm version is presented in Figure 5(a). The gain is 0 dB at approximately 2 mV and rises to its maximum value near 80 mV. This saturation occurs because, beyond a certain control voltage, the differential pair enters the limiting region where the current is fully steered to one side, and further increases in v_{cntrl} no longer affect the output. For the 90 nm version (shown in Figure 5(b)), it is seen that the gain is 0 dB at 4.6 mV and saturates to its maximum value beyond 70 mV. Thus, it is evident that the Gilbert cell allows for a significant range of gain variation (from 0 dB to its maximum value), which can be controlled precisely by v_{cntrl}.

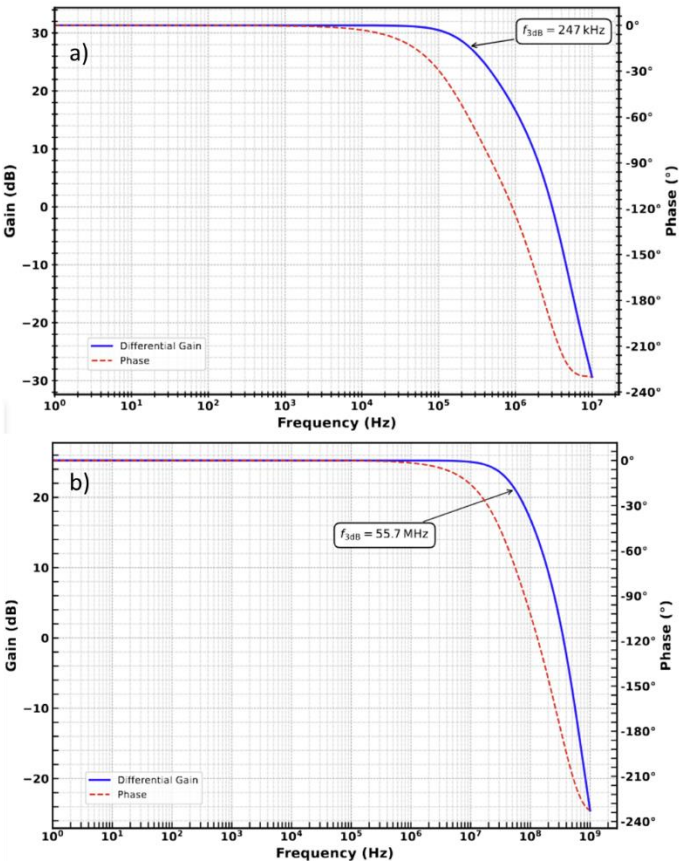

Fig. 4 Open-loop frequency response of the amplifier for (a) 45 nm node and (b) 90 nm node, respectively.

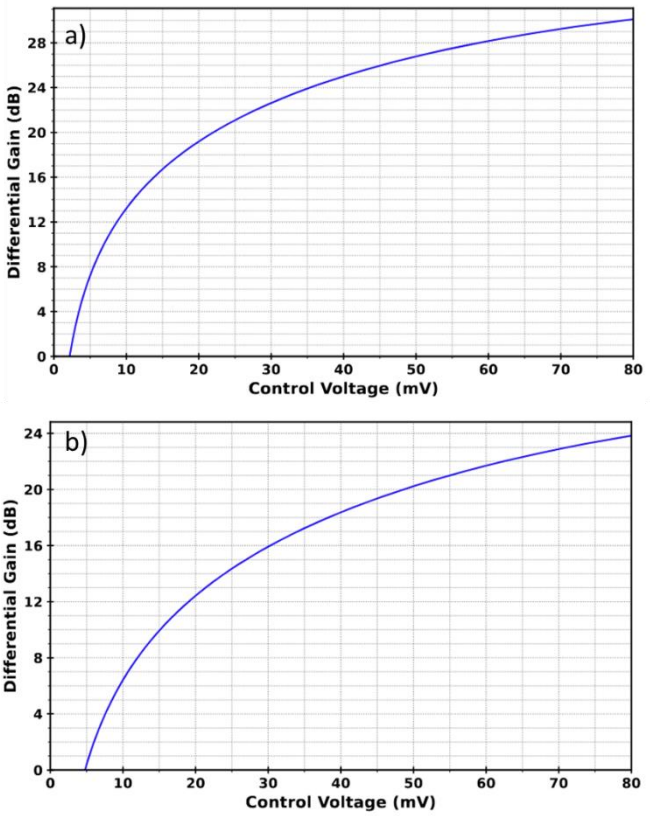

Fig. 5 Low frequency gain variation with differential control voltage for (a) 45 nm node and (b) 90 nm node, respectively.

Presented in Figure 6 is the input-referred noise of the two versions. It can be seen from Figure 6(a) that the input-referred noise for the 45 nm version decreases significantly after 100 kHz. The input-referred noise is 32 $\mu V/\sqrt{Hz}$ at 150 kHz. Beyond 500 kHz, the input-referred noise is below 2 $\mu V/\sqrt{Hz}$.

Figure 6(b) shows that the input-referred noise is below 9 $\mu V/\sqrt{Hz}$ beyond 1 MHz. At 40 MHz, it has a value of 1.7 $\mu V/\sqrt{Hz}$. This decrease in input-referred noise with frequency is expected as the flicker noise of the MOSFET has an inverse relation with frequency, as shown by Equation (11).

$$V_n^2(f) = \frac{K}{C_{ox}WL \cdot f} \tag{11}$$

Here, V_n^2(f) represents the power spectral density of the flicker noise voltage as a function of frequency f, and K is a process-dependent constant that characterizes the magnitude of flicker noise.

Additional simulated parameters include PSRR, CMRR, and slew rate. The results are summarized in Table III, which compares the two amplifier versions presented in this paper with other VGAs from the literature reviewed in our study.

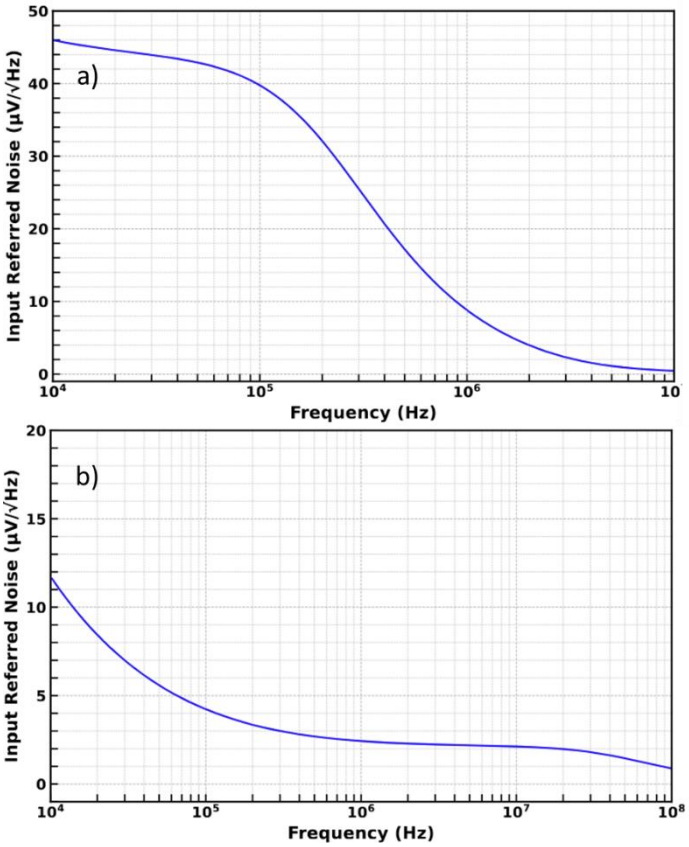

Fig. 6 Input-referred noise for (a) 45 nm node and (b) 90 nm node, respectively.

Table III Comparison of Proposed Work with Other VGA Designs from Literature

Parameter	This work (90 nm)	This work (45 nm)	Ref. [16]	Ref. [17]	Ref. [18]	Ref. [19]
Technology	90 nm	45 nm	180 nm	180 nm	180 nm	180 nm
V_{DD}	0.5 V	0.5 V	1.8 V	1.8 V	0.5 V	0.5 V
Power	1 µW	10 nW	6.5 mW	0.9 mW	70 nW	1.5 µW
Gain	25.24 dB	31.3 dB	47.5 dB	30.6 dB	77 dB	62 dB
3dB BW	55.7 MHz	274 kHz	32 MHz	10.8 MHz	0.5 Hz	80 Hz
Slew Rate	32.27 mV/µS	17.1 mV/µS	-	-	2 mV/µS	35 mV/µS
CMRR	42.21 dB	53.3 dB	-	-	55 dB	-
PSRR	16.58 dB	24 dB	-	-	52 dB	-

4. Conclusions

This work presents an ultra-low-power VGA operating at a supply voltage of 0.5 V. The circuit is based on a folded cascode topology with a Gilbert cell for gain variation. The design is biased in the subthreshold region to achieve extremely low power consumption. A comparative analysis of the proposed design was conducted for 90 nm and 45 nm technology nodes. The 45 nm implementation operates with a total current of 20 nA, consuming only 10 nW of power. It achieves a high gain of 31.3 dB with a 3 dB bandwidth of 247 kHz. The 90 nm version operates with a current of 2 µA, consuming 1 µW of power. It achieves a gain of 25.24 dB while maintaining a high 3 dB bandwidth of 55.7 MHz. In addition to this, the amplifier also offers a high slew rate, CMRR, and PSRR while offering a significant range of gain variation. These performance metrics make the proposed design well-suited for applications requiring high gain and low power, such as biomedical implants and ECG machines.

Building upon this present design, several avenues are to be explored. Future work includes a comprehensive linearity analysis of the design, which would allow for greater precision in gain control. Furthermore, design iterations using 28 nm and 22 nm CMOS technologies are to be analyzed. This would enable improvements in slew rate and a further reduction in power consumption. Biomedical implants continue to evolve to use lower power and supply voltages; thus, further design modifications will be made to allow the circuit to operate at supply voltages even below 0.5 V.

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AUTHORS:

Tanmay Deuskar is a senior-year undergraduate pursuing a Bachelor of Engineering (B.E.) in Electronics and Communication Engineering at the Birla Institute of Technology and Science, Pilani. His research interests include microelectronics, VLSI design, and analog integrated-circuit (IC) design.

E-mail: f20220248@pilani.bits-pilani.ac.in

Varun Shastry is a senior-year undergraduate pursuing a Bachelor of Engineering (B.E.) in Electronics and Communication Engineering at the Birla Institute of Technology and Science, Pilani. His professional and research interests include analog design, control theory, and applied mathematics.

E-mail: f20220399@pilani.bits-pilani.ac.in

Pankaj Arora (Senior Member, IEEE) received his M.S. and Ph.D. dual degree in Electrical Engineering from IIT Madras, Chennai, India 2016. From 2016 to 2018, he was a Post-Doctoral Researcher at the Faculty of Science, The Hebrew University, Jerusalem, Israel, where he was involved in studying the light-matter interaction at the nanoscale in photonic devices. He is an assistant professor at the Department of Electrical and Electronics Engineering, Birla Institute of Technology and Science at Pilani, India. His current research interests include plasmonics, silicon photonics, optical sensors, 2D nanomaterials, microfluidics, VLSI Design, and imaging microscopy.

Corresponding author E-mail: pankaj.arora@pilani.bits-pilani.ac.in