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Performance Comparison with variation in VDD for Planar FET, FinFET and CNFET based 6T SRAM

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ABSTRACT

Static Random Access Memory (SRAM) is a type of Random Access Memory (RAM), which makes use of latching circuitry (flip-flops) to store each bit. The term static refers to the fact that data must be periodically refreshed. SRAM is very fast and hence forms an integral part of the Embedded Cache Memory and the internal registers of a CPU. . This paper presents a performance comparison for Planar FET, FinFET, CNFET and NWFET based 6T SRAM cell. All simulations are done using HSPICE. The parameters such as Read Delay, Write Delay and Power Delay Product are considered for Performance comparison.

KEYWORDS
CNFET; FinFET; NWFET;
Power Delay Product;
Read Delay; SRAM;
Write Delay

1. INTRODUCTION

Bipolar SRAM was invented in 1963 by Robert Norman, followed by the invention of MOS SRAM in 1964 by John Schmidt, both invented at Fairchild Semiconductors. SRAM makes use of flip-flops as latching circuitry to store data. Though characterized as volatile memory, it has high data remanence. The term static refers to the fact that the data in SRAM must be periodically refreshed. SRAM offers a simple data access model and does not require a separate refresh circuit. It offers good performance and reliability, with low power consumption while idle.

With the onset of high-performance VLSI chips, efficient methods to store electronic data are required to meet the ON-chip requirement. SRAMs prove to be a good choice in such cases. They are a critical part of almost all micro-electronic devices. With the advent of technology and downsizing of transistors (as stated by Moore's Law), there has been a need for newer technologies, since CMOS fails to work on lower technology nodes. This happens because lowering of channel length beyond a certain limit leads to performance degradation with effects like Drain Induced Barrier Lowering (DIBL), Gate Induced Barrier Lowering (GIBL), Sub-threshold Leakage and many other variations in parameters. Scaling of MOSFET leads to decrease in threshold voltage (V_{Th}), thereby causing an enormous leakage current to flow. Hence, to meet the increasing demands of miniaturization and various other performance requirements, FinFETs, CNFETs and NWFETs have come into existence.

As nanometer process technologies have advanced, chip density and operating frequency have increased, making the power consumption in battery-operated portable devices a major concern. Even for non-portable devices, power consumption is a major concern because of the overall packaging and cooling cost, on top of the reliability problems.

A CNFET (Carbon Nanotube Field Effect Transistor) uses a single carbon nanotube or an array of carbon nanotubes instead of Silicon to form the channel. A carbon nanotube's diameter and chiral angle affect its bandgap, which make it a promising candidate for nano-scale transistor devices. With the fast-changing technology, it is believed that FinFETs will be out of the game soon. Hence, NWFETs, also called Gate-All-Around FETs (GAAFETs) come into picture. They can be scaled beyond 5nm, have better speed and power and are much smaller.

This paper brings forward the Performance Comparison for Planar FET, FinFET, CNFET and NWFET based 6T SRAM cell. The paper is divided into the following sections: Section II deals with the various technologies used to design the 6T SRAM cell, Section III deals with the design and function of 6T SRAM, Section IV presents the simulation results and Section V draws the attention towards the Conclusion.

2. DIFFERENT TECHNOLOGIES FOR DESIGNING 6T SRAM CELL

The technologies used to design 6T SRAM cell are:

1. Planar FET (MOSFET)
2. FinFET

3. CNFET (Carbon Nanotube FET)

The Planar FET, also known as MOSFET, is a voltage-controlled device having four terminals, namely Source, Drain, Gate and Body (or Substrate). It is a type of insulated Field-Effect Transistor. Invented in 1959, is forms a basic building block of almost all the modern electronic devices. When inappropriate voltage is applied between the gate and the source (i.e., negative in case of NMOS and positive in case of PMOS), the MOSFET is always non-conducting. Once appropriate voltage is applied, the MOSFET switches to the conducting mode.

The continuous scaling of the semiconductor devices and the increase in devices on a single chip results in more complex technology, device and circuit design. Reducing the e gate length of MOSFET brings the short channel effects into play. Thus, at short lengths, MOSFETs suffer from parameters such as threshold voltage shift, increased leakage current and increased output conductance.

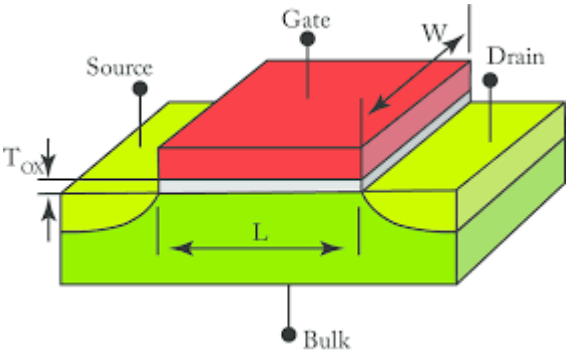

Fig. 1 Basic structure of MOSFET

The FinFET (Fin Field-effect Transistor) is a multi-gate device, consisting of a MOSFET built on a substrate where the gate is placed on two, three or four sides of the channel, forming a double gate structure. In these devices, the source and drain regions form a fin-like structure on the Silicon surface. FinFET being a 3D-strcture is significantly faster and better performing as compared to a Planar FET.

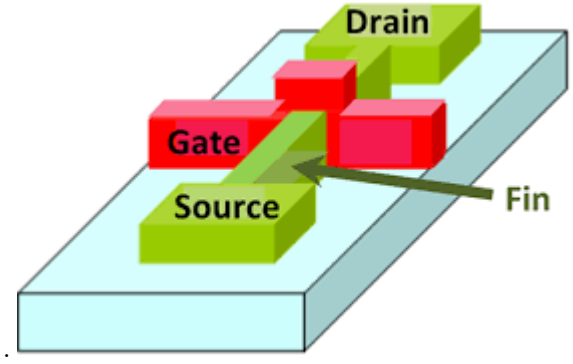

Fig. 2 Basic structure of FinFET

A CNTFET (Carbon Nanotube Field-Effect Transistor) proves to be a promising alternative to the conventional silicon technology, owing to its unique electrical properties. Carbon Nanotubes were discovered in 1991 and have seen a significant use and improvement since then. A CNTFET uses a single CNT as the channel instead of the conventionally used silicon bulk. Carbon Nanotubes are rolled up sheets of Graphene, proving to have a perfect crystalline structure with a strong C-C bond. CNTFET may be a single walled nanotube structure or a multi walled nanotube structure, depending on the number of channels used.

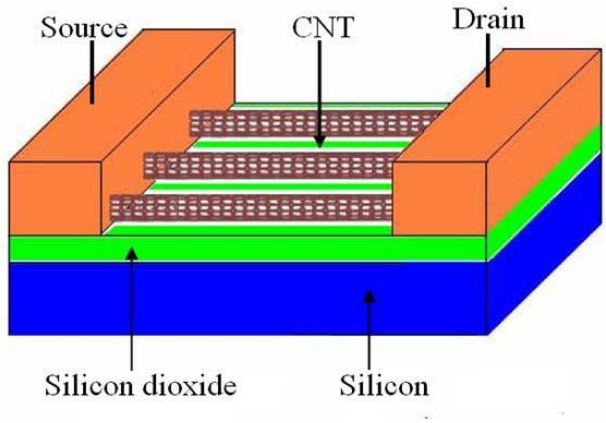

Fig. 3 Basic structure of CNTFET

Since Planar FETs are bound to reach their physical limits and hence become a saturated technology in the years to come, newer technologies like FinFETs and CNTFETs have come into existence. Planar FETs when scaled down to the nano regime suffer due to the short channel effects and observe a degradation in performance. FinFETs have a better scalability than MOSFETs, but when used beyond the 14nm node, also have certain disadvantages, like using a high dielectric material among others.

3. DESIGN OF 6T SRAM

A 6T SRAM cell is made using two cross-coupled inverters and two access transistors, connecting the cell to bit lines. The cross coupled transistors serve as the storage unit, while the access transistors are means of reading the data. The storage cells have two stable states, 0 and 1.

Access to the cell is enabled by the Word Line (WL) which controls the access transistors (M5 and M6). These are used to transfer the data for both read and write operations.

The 6T SRAM has a differential read operation, in which both the stored value and its inverse are used to determine the stored value. While reading, the Word Line (WL) is held low, thus, the two access transistors are in the OFF state. If 0 is stored in one inverter, then 1 will be stored in the other transistor.

The write operation is performed by keeping WL at 0, so that the access transistors are in the ON state. To write 0 into the storage unit, BL is kept at 0, while BL' is kept at 1.

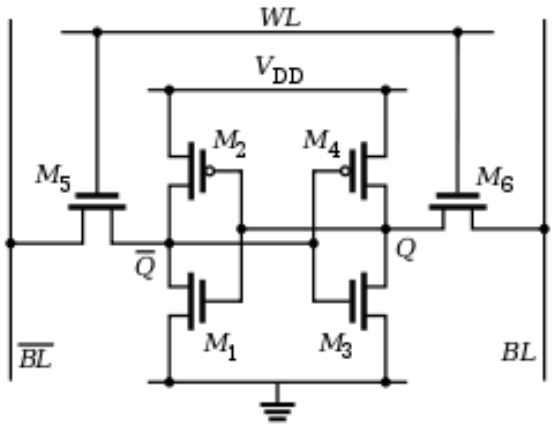

Fig. 4 Schematic of 6T SRAM

4. SIMULATION RESULTS

The circuit is simulated using HSPICE. The power of the circuit is calculated with the variation in VDD for Planar FET, FinFET and CNTFET based SRAM cell. The value of VDD has been varied from 1V to 2V.

It is observed that as the value of VDD is increased in Planar FET from 1V to 2V, i.e. power supply is doubled, the power dissipation increases by 20 times. On the other hand, the power dissipation in FinFET becomes 15 times, while that in CNTFET increases by approximately 12 times. As the value of supply voltage increases, there is an increase in the power dissipation in the circuit. While Planar FET has a large increase, the increase is relatively less in case of FinFET and the least in case of CNTFET.

VDD (in V)	Power (in µW)		
	Planar FET	FinFET	CNTFET
1	0.012	0.0060	0.0025
1.2	0.0166	0.0072	0.003
1.4	0.027	0.0108	0.0048
1.6	0.0602	0.0231	0.0112
1.8	0.124	0.0516	0.0258
2	0.248	0.0918	0.046

Table 1: Power Dissipation for various technologies

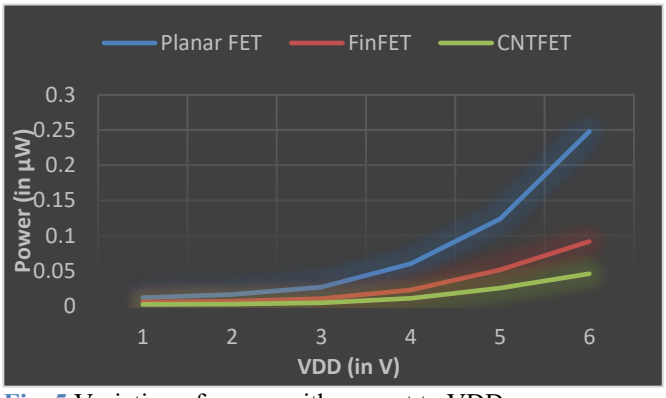

Fig. 5 Variation of power with respect to VDD

5. CONCLUSION

The work presented in this paper aim to cope up with the increasing demands of technology which is being bogged down by the power dissipation of the circuit. The work presented in the paper compares the power dissipation of a 6T SRAM cell designed using different technologies. It can be seen that the power dissipation of Planar FET (MOSFET) is nearly 2.5 times that of FinFET, while the power dissipation of FinFET is roughly 2 times that of CNTFET. With increasing demand for miniaturization of the circuit and reduced power dissipation, the CNTFET 6T SRAM proves to be an efficient storage circuit.

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